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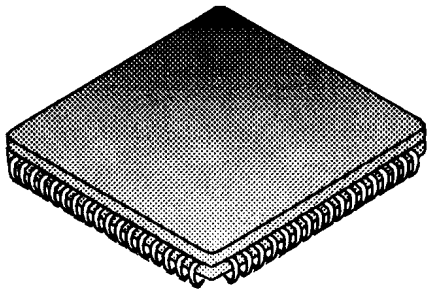
DSP56401

AES/EBU/CP340 Digital Audio Transceiver



Plastic Leaded Chip Carrier (PLCC)
Available in a 68 pin, small footprint package for surface mounting or in socket

The DSP56401 is a low cost, digital audio transceiver system which is compatible with the AES/EBU and EIAJ CP340 digital audio transmission standards. These standards are supported by CD players, RDAT recorders, professional recording and broadcasting equipment, audio workstations, and an ever-increasing variety of other audio equipment. The DSP56401 is also useful in applications using RDAT recorders as mass storage for general data. Each on-chip function (transmit serial interface, transmit modulator, receive demodulator, receive serial interface, and clock generation and control) is independent and asynchronous with the other functions. The modulator and demodulator sections include oscillators to set the transmit frequency and a phase locked loop (PLL) to recover the receive bit, frame and block synchronization. The serial interfaces provide a no-glue interface to Motorola DSP SSI and SCI ports, 6805 and 68HC11 SPI ports, and Motorola Sigma-Delta A/D and D/A converters. The level of the DSP56401's user features is controlled primarily by software drivers. A minimum system may use only audio sample data, while a professional system may also need to manipulate non-audio data in real-time. The DSP56401 also provides system controller functions, such as clock generation and serial bus management, under DSP software control. Eight serial modes provide flexible interfacing for the audio sample data and the non-audio information in various systems.

Features

- Single chip digital audio system - transmitter, receiver and clock generation.
- Compatible with the AES/EBU and EIAJ CP340 digital audio transmission standards.
- Allows simple audio-only data interfaces or full-featured AES/EBU systems.
- Independently clocked on-chip transmitter, receiver and serial interfaces.
- Four on-chip oscillators with on-chip programmable dividers.
- On-chip phase locked loop frequency and phase detectors.
- Three software selected digital audio inputs
- Two programmable clock outputs
- Four programmable I/O pins.
- No-glue interface to Motorola DSP SSI, I^2S and Japanese digital audio interfaces.
- No-glue interface to Motorola DSP SCI and MCU SPI ports for non-audio data.
- Serial daisy-chain supports digital audio buses having multiple DSP56401 and data converter time slots.
- Simultaneous stereo sampling with two Motorola DSP56ADC16 A/D converters.
- Low jitter clock recovery compatible with Sigma-Delta converter requirements.
- Multi-Port Serial Interface™ provides eight serial data formats.
- Programmable number of 16, 24 or 32 bit serial time slots.
- All non-audio information is available at fast or slow transfer rates.
- Non-audio data interface supports SSI, SCI, SPI, and EPROM ports.
- User features and DSP software loading controlled by software drivers.
- 24 bit program word and 16 bit status word control and monitor on-chip operation.
- Hardware parity generation and error detection.
- Hardware CRC generation and error detection.
- Multiple chip transmit modulator synchronization.
- TTL compatible inputs, CMOS compatible outputs.
- Low cost 68 pin PLCC (plastic leaded chip carrier) surface mount package.

Multi-Port Serial Interface is a trade mark of Motorola Inc.

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DSP sales and Marketing (512) 891-2030

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9600/4800/2400/1200/300 baud
(512) 891-DSP3
(8 data bits, no parity, 1 stop)

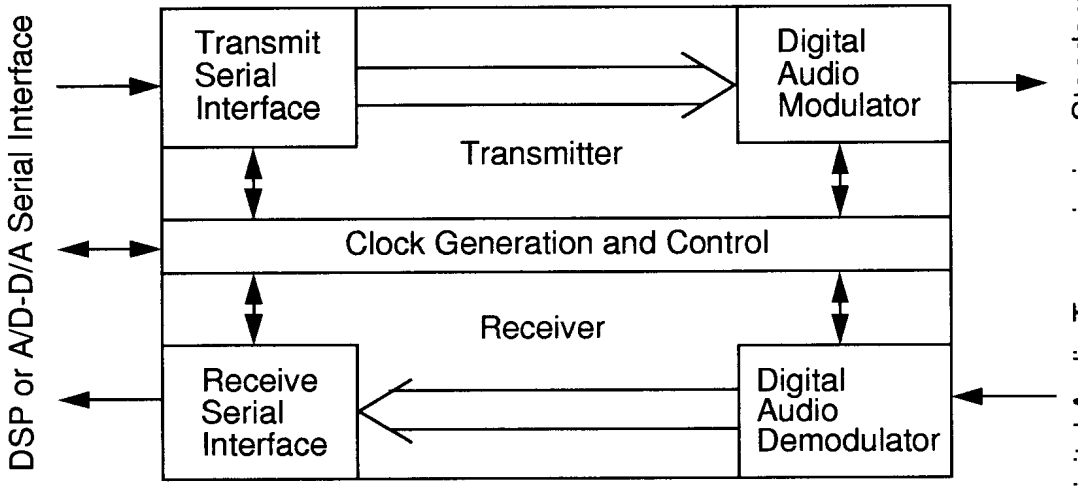


Figure 2-1 Functional Block Diagram

Block Diagram Description

A functional block diagram of the DSP56401 is shown in Figure 2-1. The chip consists of an independent transmitter and receiver with common clock generation and control logic. The transmitter consists of a digital audio modulator and a serial interface, and the receiver consists of a digital audio demodulator and a serial interface. The transmitter and receiver may have independent, asynchronous clocks or may be clocked together. Similarly, the serial interfaces may be clocked asynchronously with respect to the modulator, demodulator or each other. Internal synchronizers resample signals passing between sections.

2.1 Transmit Serial Interface

A block diagram of the transmit serial interface is shown in Figure 2-2. The transmit serial interface provides serial inputs for audio sample data, non-audio data and control information. Audio data is transferred in a most significant bit (MSB) first format compatible with the default mode of Motorola's DSP56000/DSP56001 family. The data format and pin usage are controlled by the serial mode. Eight serial modes allow a wide variety of interface options, including 16- or 24-bit audio samples, fast or slow non-audio data, and time-multiplexed, serial networks with 16-, 24- or 32-bit time slots. The Multi-Port Serial Interface™ provides

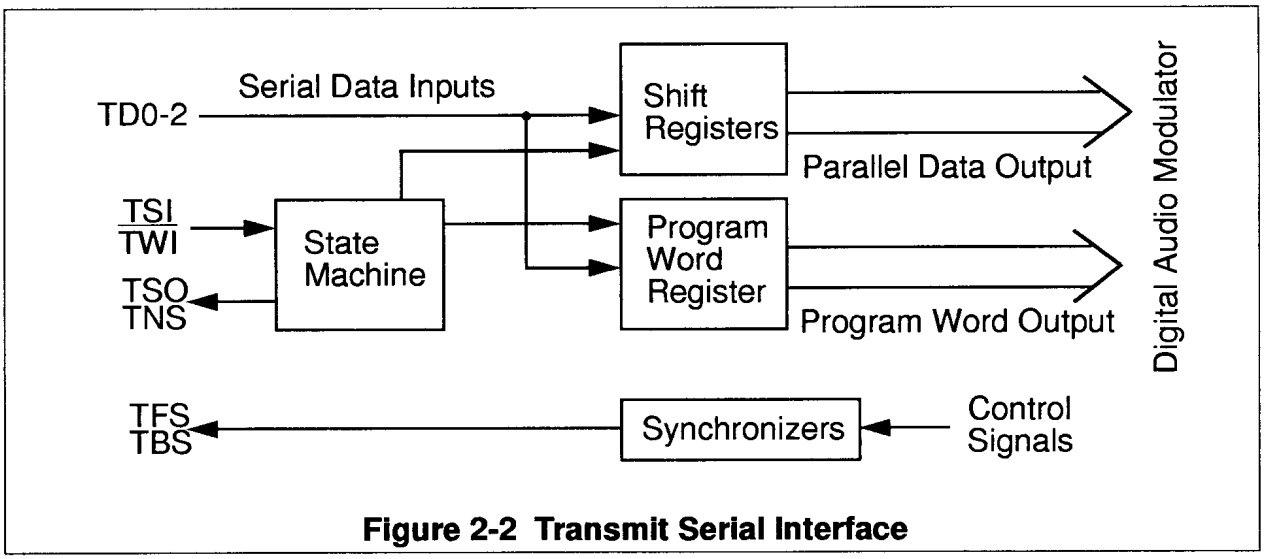


Figure 2-2 Transmit Serial Interface

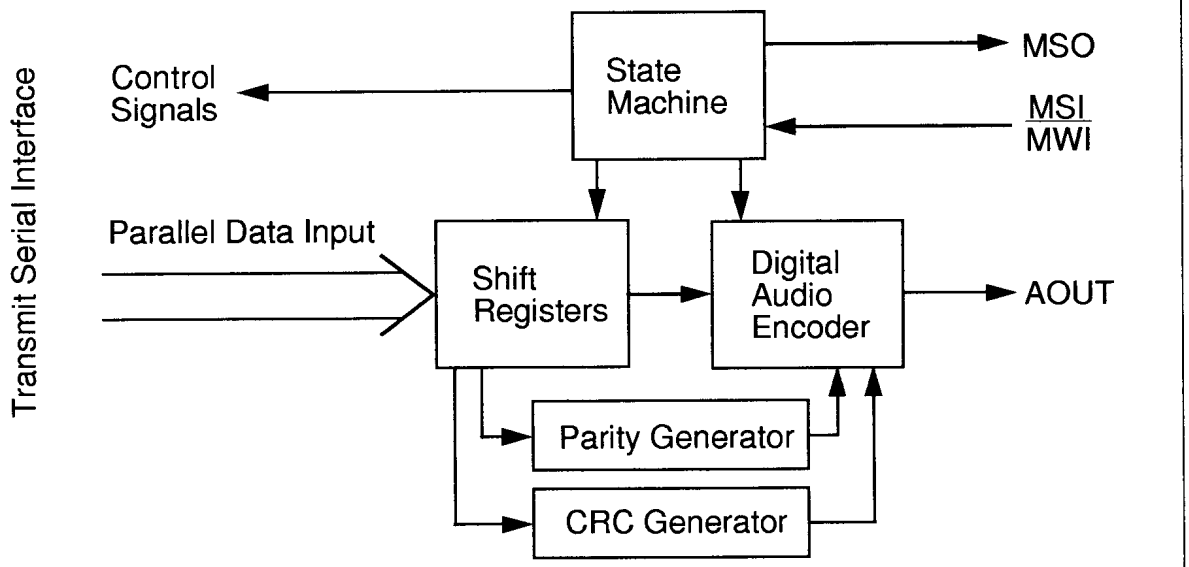


Figure 2-3 Digital Audio Modulator

multiple input bit streams and supports Motorola SSI, SCI and SPI protocols. The serial input format repeats once per sample period (frame). Buffered data is transferred in parallel once per frame to the digital audio modulator and is converted to least significant bit (LSB) first representation to match the AES/EBU/CP340 standard during this transfer.

2.2 Digital Audio Modulator

A block diagram of the digital audio modulator is shown in Figure 2-3. The modulator produces an LSB first, serial data output compatible with the AES/EBU/CP340 digital audio transmission standard. The modulator state machine generates preambles, parity and, optionally, CRC information which are added to the frame of audio sample data and non-audio data received from the transmit serial interface.

2.3 Digital Audio Demodulator

A block diagram of the digital audio demodulator is

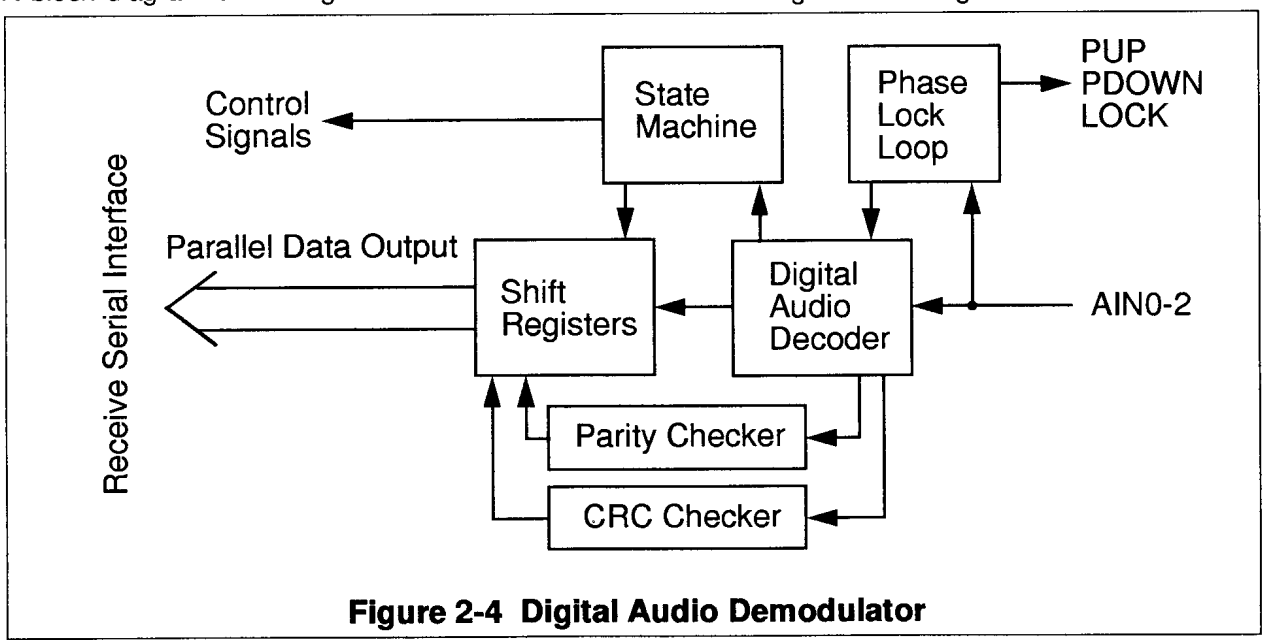


Figure 2-4 Digital Audio Demodulator

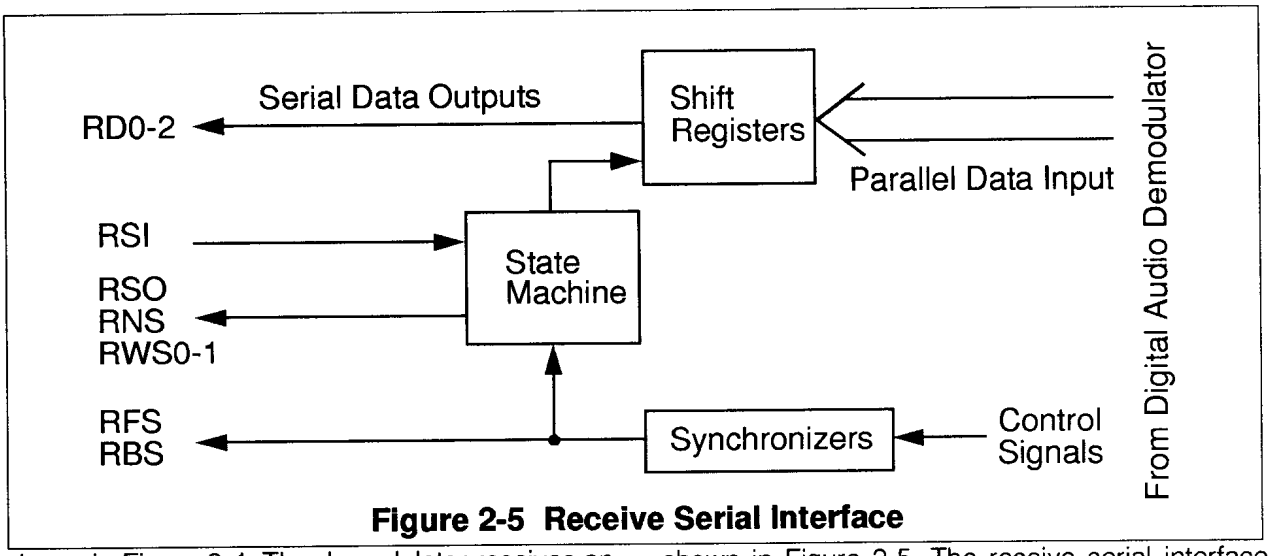


Figure 2-5 Receive Serial Interface

shown in Figure 2-4. The demodulator receives an LSB first serial data input compatible with the digital audio transmission standard. The demodulator PLL recovers a bit clock from the modulated serial input. The demodulator state machine detects preamble sync patterns, parity errors and CRC errors, and separates the audio sample data from the non-audio data. The separated data is converted to MSB first representation during a parallel transfer once per frame to the receive serial interface.

2.4 Receive Serial Interface

A block diagram of the receive serial interface is shown in Figure 2-5. The receive serial interface provides an MSB-first serial output for audio sample data, non-audio data and status information. The data format and pin usage are controlled by the serial mode. Eight serial modes allow a wide variety of interface options, including 16- or 24-bit audio samples, fast or slow non-audio data, and time-multiplexed, serial networks with 16-, 24- or 32-bit time slots. The Multi-Port Serial Interface™ provides multiple output bit streams and supports Motorola SSI, SCI and SPI protocols. A frame of buffered serial output data repeats its format once per frame.

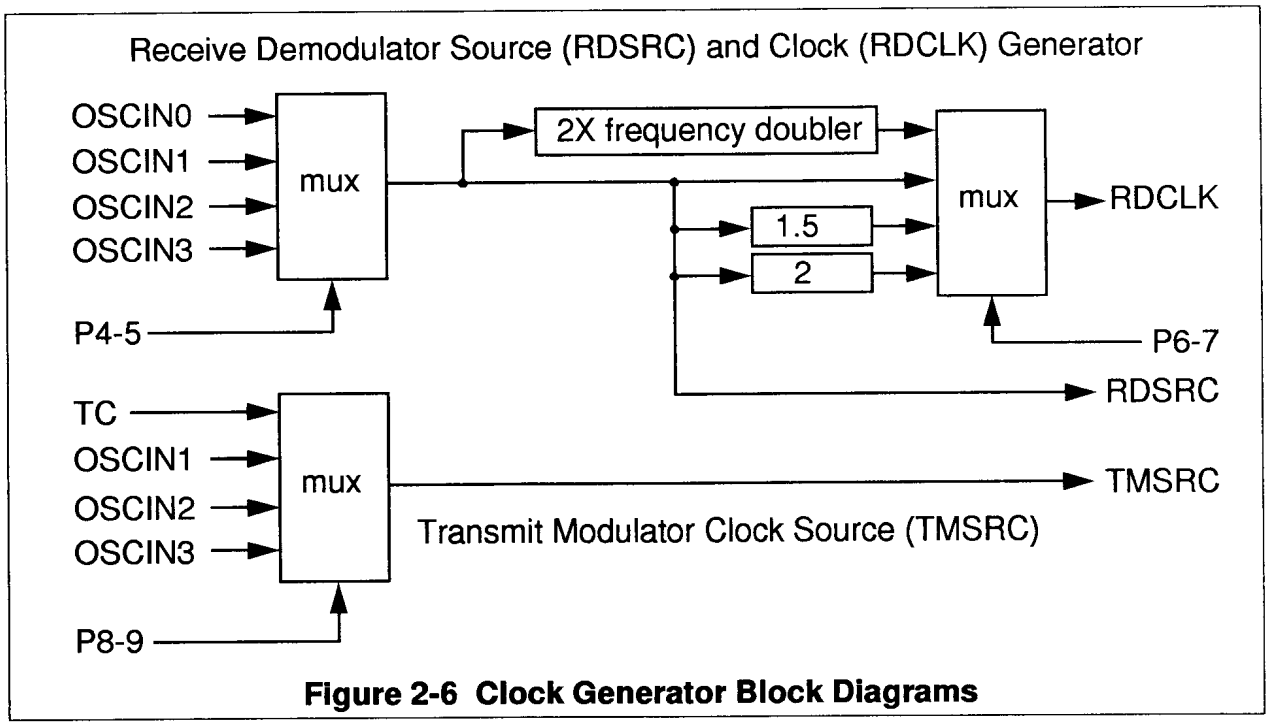


Figure 2-6 Clock Generator Block Diagrams

2.5 Clock Generation and Control

The clock generator provides four general purpose oscillators which may be used as fixed frequency oscillators for the transmitter or as variable frequency, voltage controlled oscillators for the receiver PLL. Control logic supplies these clocks via programmable dividers to all chip functions. Figure 2-6 and Figure 2-7 are block diagrams of the clock generator logic, which is software controlled. A 24-bit program word (P0-P23) is loaded through the transmit serial interface and controls most chip options. A 16-bit status word (S0-S15) is read out through the receive serial interface and allows the user to monitor chip operation. The TMCLK clock generator contains phase adjustment circuits which permit synchronization of multiple transmit modulators.

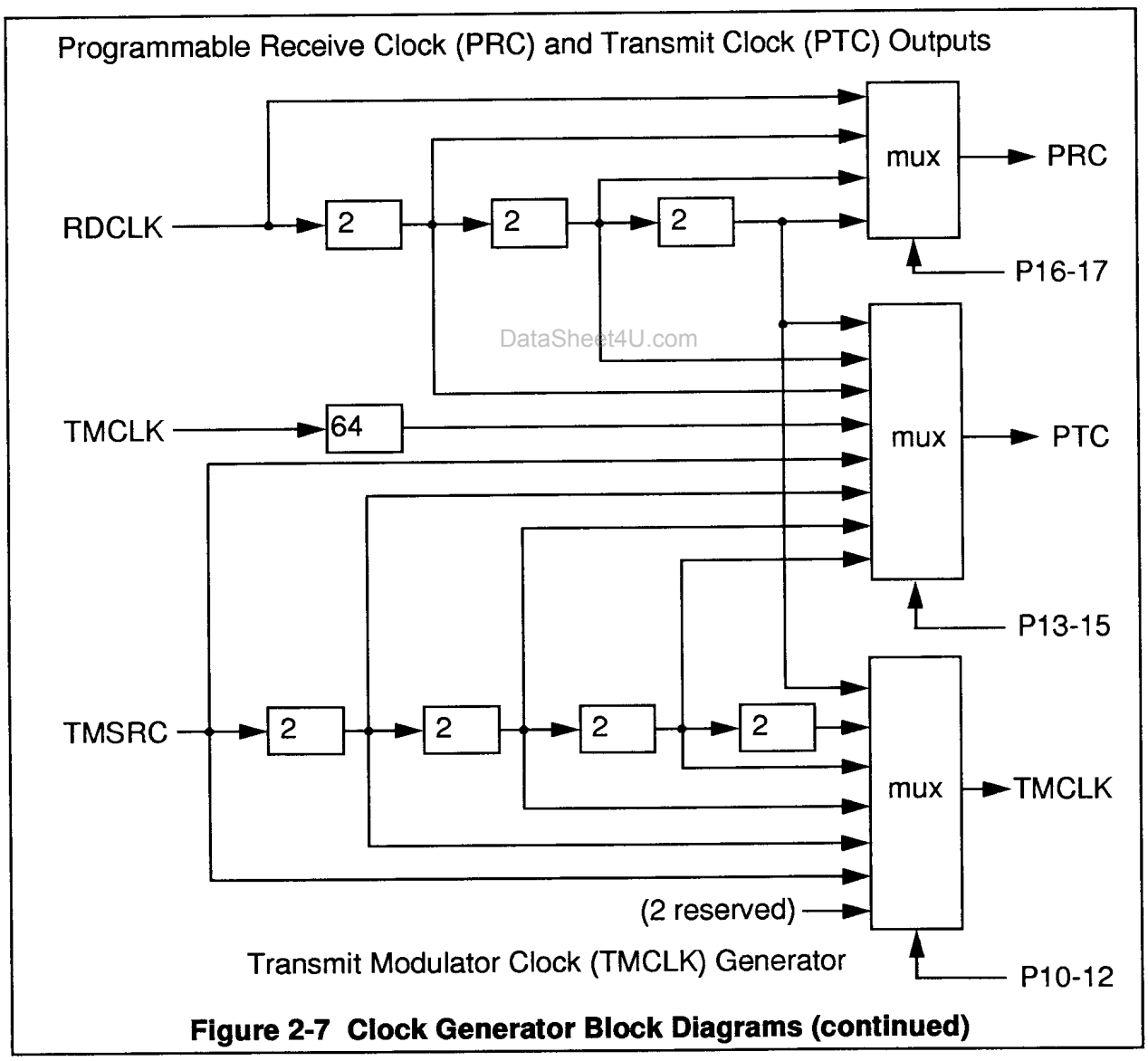


Figure 2-7 Clock Generator Block Diagrams (continued)

Signal Descriptions

The DSP56401 is packaged in an industry standard, 68 pin plastic leaded chip carrier (PLCC) having the pinout shown in Figure 3-1. A functional view of the DSP56401 pinout is shown in Figure 3-2. These signals are arranged into five functional groups — transmit serial interface, digital audio modulator, digital audio demodulator, receive serial interface, and clock generation and control.

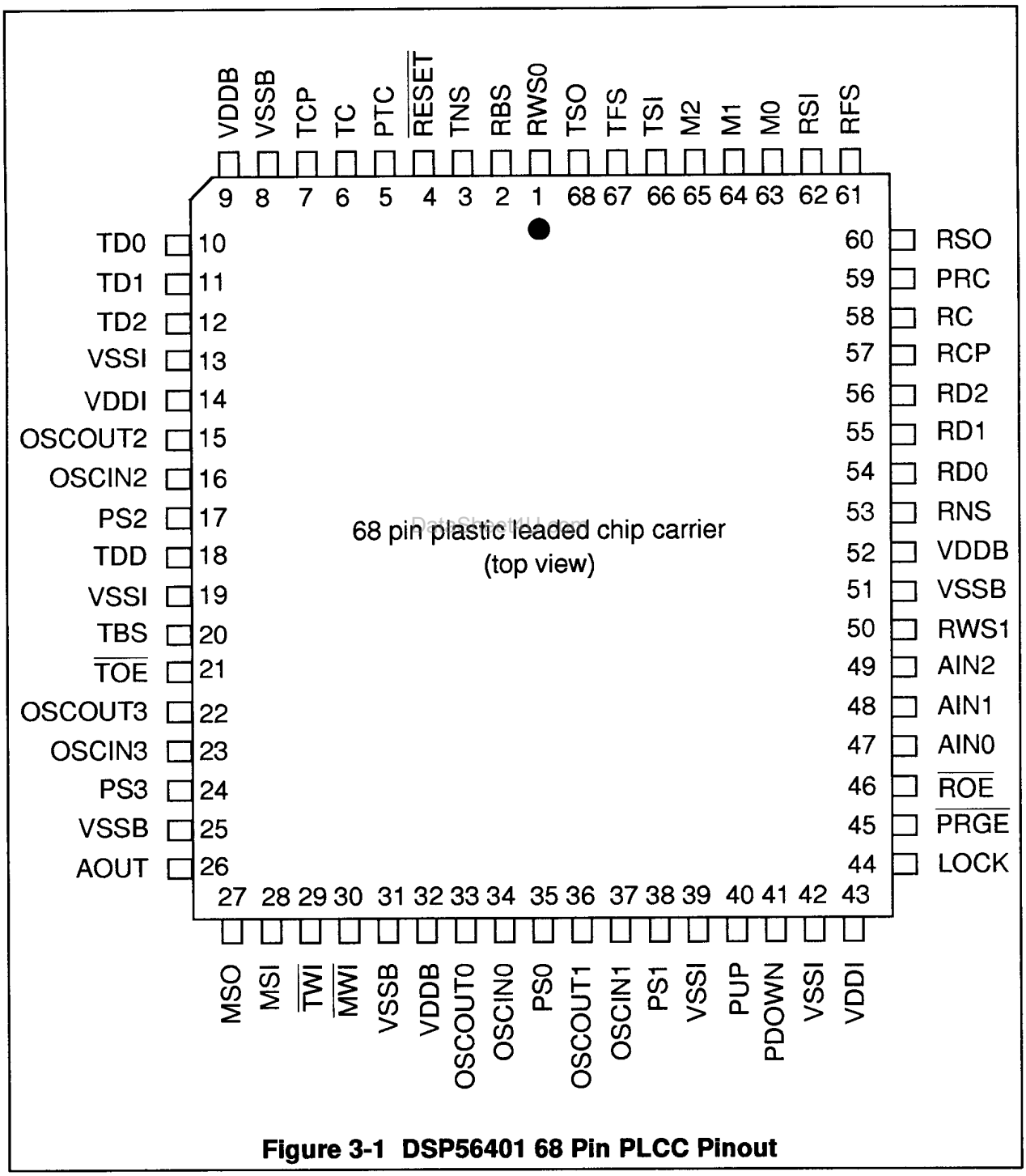


Figure 3-1 DSP56401 68 Pin PLCC Pinout

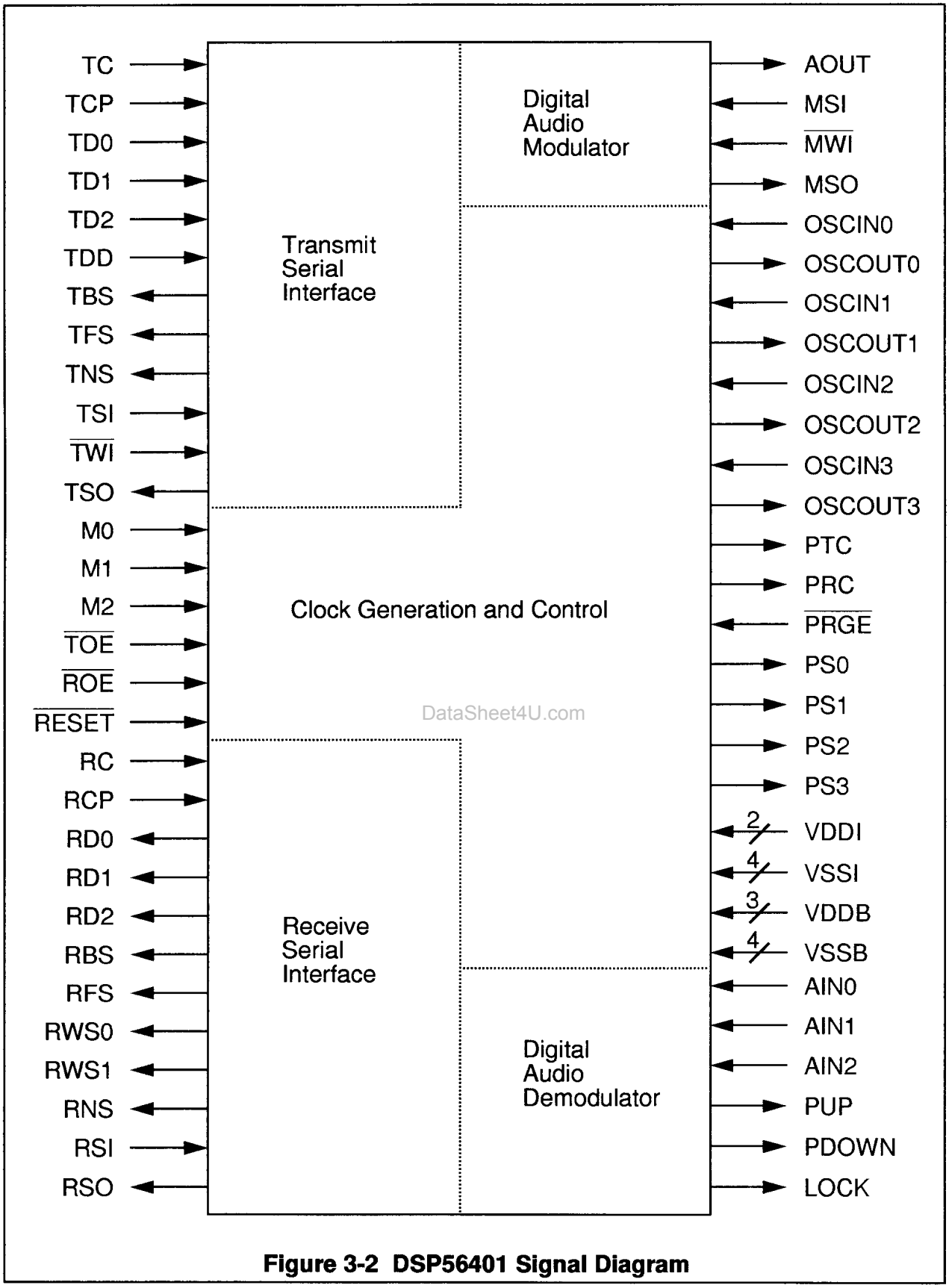


Figure 3-2 DSP56401 Signal Diagram

3.1 Transmit Serial Interface Signals

3.1.1 TC (Transmit Serial Clock: Active High Input)

This input is the transmit serial interface bit clock. TC may be asynchronous to RC and OSCIN0-3. However, some applications may require TC to be synchronized with other clocks. At least 32 TC clocks per frame sync are required for proper operation.

3.1.2 TCP (Transmit Clock Polarity: Active High Input)

This input is exclusive ORed with TC to generate the internal transmit serial bit clock. If TCP is low, the TC clock input is unchanged. If TCP is high, the TC clock input is inverted. The sampling edge of TC is the falling edge if TCP=0 and is the rising edge if TCP=1. TCP should normally be hard-wired low or high for a particular application.

3.1.3 TD0 (Transmit Data 0: Active High Input)

This input receives serial audio data each transmit sample period (frame). In Modes 3 and 7, TD0 ignores any input until TSI is asserted or $\overline{TWI}$ changes. If TDD=0, active input sampling begins one bit period after TSI or $\overline{TWI}$ is asserted, and it ends in the same bit period where TSO is asserted. If TDD=1, active input sampling begins during the same bit period that TSI goes high or $\overline{TWI}$ changes, and it ends in the bit period prior to TSO assertion. The number of serial bits and their order in each frame are defined by the serial mode pins M0-M2. Input data is sampled synchronous to the sampling edge of TC and typically changes on the non-sampling edge of TC.

3.1.4 TD1 (Transmit Data 1: Active High Input)

This input receives serial audio data each transmit sample period (frame). TD1 ignores any input until TSI is asserted or $\overline{TWI}$ changes. If TDD=0, active input sampling begins one bit period after TSI or $\overline{TWI}$ is asserted, and it ends in the same bit period where TSO is asserted. If TDD=1, active input sampling begins during the same bit period that TSI goes high or $\overline{TWI}$ changes, and it ends in the bit period prior to TSO assertion. TD1 ignores any input following the bit period where TSO is asserted. The number of serial bits and their order in each frame are defined by the serial mode pins M0-M2. Input data is sampled synchronous to the sampling edge of TC and typically changes on the non-sampling edge of TC.

3.1.5 TD2 (Transmit Data 2: Active High Input)

This input receives serial non-audio data each transmit sample period (frame) in modes 1,3,5,6 and 7. It is not used in modes 0, 2 or 4.

If the DSP56401 is operating in modes 1, 3, 5 or 7, then TD2 behaves as follows. TD2 ignores any input until TSI or $\overline{TWI}$ is asserted, beginning active input sampling after TNS changes. TD2 samples every two or four TC periods, depending on the serial mode chosen. Input data is sampled synchronous to the non-sampling edge of TC associated with each TNS rising edge and typically changes on the falling edge of TNS.

If the DSP56401 is operating in serial mode 6 (M2=1, M1=1, M0=0), then TD2 behaves as follows. TD2 ignores any input until TSI or $\overline{TWI}$ is asserted. If TDD=0, active input sampling begins one bit period after TSI or $\overline{TWI}$ is asserted. If TDD=1, active input sampling begins during the same bit period that TSI goes high or $\overline{TWI}$ changes. TD2 is sampled for eight bits, ignoring any input following these bits. These following bits should be set to zero for compatibility with future versions of the DSP56401, which may use them. Input data is sampled synchronous to the sampling edge of TC and typically changes on the non-sampling edge of TC.

3.1.6 TDD (Transmit Data Delay: Active High Input)

This input is used to delay the transmit serial interface audio data inputs. If TDD=0, the TD0 and TD1 data inputs are not affected. If TDD=1, the TD0 and TD1 data inputs are delayed by one TC clock

period. If the DSP56401 is operating in serial modes 1, 3, 5, or 7, TDD does not affect TD2. TD2 is not used in serial modes 0, 2, or 4. However, if the DSP56401 is operating in serial mode 6 (M2=1, M1=1, M0=0) and TDD=1, the TD2 data input is delayed by one TC clock period. It is not affected if TDD=0 in serial mode 6. TDD is used to skew the audio data relative to the transmit serial interface frame sync signals. Typically, TDD=0 for SSI and I^2S interfaces and TDD=1 for Burr-Brown and Japanese interfaces. TDD should normally be hard-wired low or high in a given implementation.

3.1.7 TBS (Transmit Block Sync: Three-State Output)

This output is asserted high during the last frame of each transmit block period; otherwise it is low. The first transmit data frame in the block is input by the transmit serial interface in the frame period following TBS high, thus TBS is an end of block indicator. TBS is derived by sampling the modulator preamble generation and synchronizing the event to TC. TBS changes synchronous to the non-sampling edge of TC during the same TC period that TFS goes low and is stable on the sampling edge of TC. If TC is not synchronous to the modulator clock, TBS may jitter due to asynchronous sampling. For jitter-free TBS operation, both TC and the transmit modulator should be driven by a common clock. This requirement can be met by driving TC from PTC or PRC programmed as a transmit modulator clock output, or as a receive demodulator clock output if the transmit modulator is locked to the receive demodulator. TBS is high impedance when $\overline{\text{RESET}}$ is asserted or $\overline{\text{TOE}}$ is deasserted.

3.1.8 TFS (Transmit Frame Sync: Three-State Output)

This output is asserted high for one TC period of each transmit sample period (frame); otherwise it is low. TFS is derived by sampling the modulator preamble generation and synchronizing the event to TC. TFS changes synchronous to the non-sampling edge of TC and is stable on the sampling edge of TC. If TC is not synchronous to the modulator clock, TFS may jitter due to asynchronous sampling. For jitter-free TFS operation, both TC and the transmit modulator should be driven by a common clock. This requirement can be met by driving TC from PTC or PRC programmed as a transmit modulator clock output, or as a receive demodulator clock output if the transmit modulator is locked to the receive demodulator. TFS is high impedance when $\overline{\text{RESET}}$ is asserted or $\overline{\text{TOE}}$ is deasserted.

3.1.9 TNS (Transmit Non-Audio Sync: Three-State Output)

TNS is a gated clock output used to transfer non-audio data at a slower rate than its associated audio sample data. Non-audio data consists of

Table 3-1 TNS Parameters

Serial Mode	TNS Period	TNS Width	----- Relative to TSI or TWI Assertion -----		
			TNS Start	TNS End	TNS Driven
0	4TC	2TC	32TC	62TC	1-72TC
1	4TC	2TC	8TC	38TC	1-48TC
2	4TC	2TC	24TC	54TC	1-64TC
3	2TC	TC	7TC	22TC	1-32TC
4	4TC	2TC	8TC	38TC	1-48TC
5	2TC	TC	7TC	22TC	1-32TC
6	4TC	2TC	8TC	38TC	1-48TC
7	2TC	TC	7TC	22TC	1-32TC

eight bits (one byte) per sample period (frame). TNS is high impedance until TSI or $\overline{TWI}$ is asserted, becoming active synchronous to the next non-sampling edge of TC. TNS remains active until TSO is asserted, becoming high impedance synchronous to the next non-sampling edge of TC. Since TNS is high impedance during inactive time slots, an external pullup resistor is required in the system. TNS consists of eight active low clock pulses per frame, each pulse having a width of one or two TC clocks and a clock period of two or four TC clocks, depending on the serial mode selected (using the serial mode pins M0-M2). The first TNS pulse is delayed a varying number of TC clocks after TSI or $\overline{TWI}$ is asserted, depending on the serial mode. See Table 3-1 for more information. The last TNS pulse ends ten TC clocks before TSO is asserted, independent of the serial mode. TNS changes synchronous to the non-sampling edge of TC and is stable on the sampling edge of TC. TNS may be used to directly interface non-audio data from a DSP56000 family SCI in shift register mode, a 6805 or 68HC11 SPI, or a parallel-to-serial converter. TNS is high impedance when $\overline{RESET}$ is asserted.

3.1.10 TSI (Transmit Sync In: Active High Input)

This input is asserted high for one TC period of each transmit sample period (frame) to begin transmit data transfer; otherwise it is low. TSI assertion defines a start of frame event. If TDD=0, the first transmit audio data bit is sampled one TC bit period after TSI is asserted. If TDD=1, the first transmit audio data bit is sampled in the same TC bit period that TSI is asserted. For a single serial device, TSI is typically connected to TFS. For multiple, time-multiplexed serial devices, TSI and TSO form a daisy-chain which defines transmit data time slots for each serial device. In a transmit daisy-chain, TSI is typically connected to TSO of the serial device occupying the previous transmit time slot(s) or to TFS if the device occupies the first transmit time slot. If TSI is asserted before TSO is asserted, the current data transfer is ignored (lost) and a new data transfer is started. TSI must meet setup and hold times synchronous to the sampling edge of TC, and typically changes on the non-sampling edge of TC. TSI and $\overline{TWI}$ are internally combined to create the start of frame signal. If TSI is not used, it should be tied low.

3.1.11 $\overline{TWI}$ (Transmit Word In: Active Low Input)

This input is asserted low each transmit sample period (frame) to begin transfer of the channel A audio sample and is deasserted high each transmit sample period to begin transfer of the channel B audio sample. $\overline{TWI}$ assertion defines a start of frame event and $\overline{TWI}$ deassertion defines a middle of frame event. If TDD=0, the first transmit audio data bit is sampled one TC bit period after $\overline{TWI}$ is asserted. If TDD=1, the first transmit audio data bit is sampled in the same TC bit period that $\overline{TWI}$ is asserted. When the middle of the frame is reached, the internal state machine looks for $\overline{TWI}$ deassertion. If $\overline{TWI}$ is not deasserted, the transmit serial interface will freeze (ignoring all TC clocks) until $\overline{TWI}$ is deasserted. If TDD=0, the middle of frame transmit audio data bit m is sampled one TC bit period after $\overline{TWI}$ is deasserted. If TDD=1, the middle of frame transmit audio data bit m is sampled in the same TC bit period that $\overline{TWI}$ is deasserted.

For stereo applications, $\overline{TWI}$ is a left/right channel indicator. If TDD=0, $\overline{TWI}$ is a left/right word clock input according to the I^2S convention. If TDD=1, an inverted $\overline{TWI}$ is a left/right word clock input according to the Burr-Brown and Japanese convention. $\overline{TWI}$ must meet setup and hold times synchronous to the sampling edge of TC, and typically changes on the non-sampling edge of TC. Note that the $\overline{TWI}$ deassertion is ignored in serial modes 3 and 7. $\overline{TWI}$ and TSI are internally combined to create a start of frame signal. If $\overline{TWI}$ is not used, it should be tied high. See Table 3-2 for more information.

3.1.12 TSO (Transmit Sync Out: Active High Output)

TSO is asserted high for one TC period in each transmit sample period (frame); otherwise it is low.

TSO follows TSI assertion by a fixed number of TC clock periods defined by the serial mode pins M0-M2. TSO follows $\overline{TWI}$ deassertion by a fixed number of TC clock periods defined by the serial mode, regardless of whether the internal state machine waits for $\overline{TWI}$ deassertion or not. See Table 3-3 for more information. For a single serial device, TSO is typically not connected. For multiple, time-multiplexed serial devices, TSI and TSO form a daisy-chain which defines transmit data time slots for each serial device. In a transmit daisy-chain, TSO is typically connected to TSI of the serial device occupying the following transmit time slot(s). TSO changes synchronous to the non-sampling edge of TC and is stable on the sampling edge of TC.

3.2 Digital Audio Modulator Signals

3.2.1 AOUT (Audio Out: Active High Output)

This output supplies audio sample data and non-audio information modulated according to the AES, EBU and CP340 digital audio transmission protocols (See Appendix B for more information on these related standards). AOUT swings to typical CMOS voltage levels and an external line driver is usually needed for AES/EBU or balanced CP340 transmission. Unbalanced CP340 calls for a signal swing of 0.5v p-p, so for very short transmission cable lengths, a resistor divider may enable a designer to meet the signal level specifications of CP340 without using an external device. Note that this does not meet the impedance specifications of CP340 and also that longer transmission lengths will require an appropriate line driver. See Sections 8.1.2 and 8.1.4 for more information. Since AOUT is biphase mark encoded, it changes on both edges of the transmit modulator clock (TMCLK).

3.2.2 MSI (Modulator Sync In: Active High Input)

This input resets the transmit modulator state machine to the start of a frame. MSI may be asserted high for one TMSRC period of each transmit sample period (frame) to transmit the first bit of the channel A sample data; otherwise it is low. The first bit of the channel A sample data is transmitted 1.5 TMCLK + 0.5 TMSRC periods after MSI is asserted. For a single serial device, MSI is typically tied low, allowing the transmit modulator to free-run and create its own frame sync. MSI may be connected to TSI to slave lock the transmit modulator to the transmit serial interface. For multiple, time-synchronized transmit modulators, MSI of each of the slave modulators is typically connected to MSO of the master transmit

Table 3-2 $\overline{TWI}$ Parameters

Serial Mode	First Frame Bit After $\overline{TWI}$ Assertion	First Possible Frame Bit After $\overline{TWI}$ Deassertion
0	1 (TDD=0), 2 (TDD=1)	25 (TDD=0), 26 (TDD=1)
1	1 (TDD=0), 2 (TDD=1)	25 (TDD=0), 26 (TDD=1)
2	1 (TDD=0), 2 (TDD=1)	33 (TDD=0), 34 (TDD=1)
3	1 (TDD=0), 2 (TDD=1)	ignored
4	1 (TDD=0), 2 (TDD=1)	17 (TDD=0), 18 (TDD=1)
5	1 (TDD=0), 2 (TDD=1)	17 (TDD=0), 18 (TDD=1)
6	1 (TDD=0),2 (TDD=1)	25 (TDD=0), 26 (TDD=1)
7	1 (TDD=0),2 (TDD=1)	ignored

modulator. MSI can also be driven by MSO of the same chip. If MSI is asserted before MSO is asserted, the current transmit frame is truncated and a new transmit frame is started. MSI should never be driven by TFS or RFS. MSI must meet setup and hold times synchronous to the sampling edge of TMSRC, and typically changes on the non-sampling edge of TMSRC. TMSRC is selected by program bits P8-P9. If the transmit modulator is locked to the receive demodulator (P10-12=000), MSI is ignored. When PTC or TMCLK is sourced from a divided-down TMSRC, that clock is phase adjusted by MSI to automatically align its rising edge with the TMSRC rising edge that follows the MSI assertion. Since divided down versions of TMSRC are phase adjusted by MSI, the transmit divider chain (via the PTC output - refer to Figure 2-7) should not be used to generate the MSI input or erratic operation will result. However, the RDCLK receive clock generator is not phase adjusted by MSI, so the receive divider chain (via the PTC or PRC outputs) may be used to generate the MSI input. MSI and $\overline{\text{MWI}}$ are internally combined to create a start of frame signal. If MSI is not used, it should be tied low.

3.2.3 $\overline{\text{MWI}}$ (Modulator Word In: Active Low Input)

This input is asserted low once each transmit sample period (frame) to reset the transmit modulator state machine to the start of a frame. The first bit of the channel A sample data is transmitted 1.5 TMCLK + 0.5 TMSRC periods after $\overline{\text{MWI}}$ is asserted. For a single serial device, $\overline{\text{MWI}}$ is typically tied high, allowing the transmit modulator to free-run and create its own frame sync. $\overline{\text{MWI}}$ may be connected to TWI to slave lock the transmit modulator to the transmit serial interface. For multiple time-synchronized transmit modulators, $\overline{\text{MWI}}$ is typically driven by a studio master sample clock. $\overline{\text{MWI}}$ should never be driven by MSO or RWS0-1. If $\overline{\text{MWI}}$ is asserted before MSO is asserted, the current transmit frame is truncated and a new transmit frame is started. $\overline{\text{MWI}}$ must meet setup and hold times synchronous to the sampling edge of TMSRC and typically changes on the non-sampling edge of TMSRC. TMSRC is selected by program bits P8-P9. If the transmit modulator is locked to the receive demodulator (P10-12=000), $\overline{\text{MWI}}$ is ignored. When PTC or TMCLK is sourced from a divided-down TMSRC, that clock is phase adjusted by $\overline{\text{MWI}}$ to automatically align its rising edge with the TMSRC rising edge that follows the $\overline{\text{MWI}}$ assertion. Since divided down versions of TMSRC are phase

Table 3-3 Delay from TSI to TSO Assertion

Serial Mode	TSO Assertion Delay from TSI Assertion	TSO Assertion Delay from TWI Deassertion
0	72TC	48TC
1	48TC	24TC
2	64TC	32TC
3	32TC	not applicable
4	48TC	32TC
5	32TC	16TC
6	48TC	24TC
7	32TC	not applicable

adjusted by $\overline{MWI}$, the transmit divider chain (via the PTC output - refer to Figure 2-7) should not be used to generate the $\overline{MWI}$ input or erratic operation will result. However, the RDCLK receive clock generator is not phase adjusted by $\overline{MWI}$, so the receive divider chain (via the PTC or PRC outputs) may be used to generate the $\overline{MWI}$ input. MSI and $\overline{MWI}$ are internally combined to create a start of frame signal. If $\overline{MWI}$ is not used, it should be tied high.

3.2.4 MSO (Modulator Sync Out: Three-State Output)

This output indicates the start of a transmit modulator frame. It may be used to synchronize transmit modulators in multiple DSP56401 systems. MSO is asserted high for one TMSRC period during the channel A preamble of each transmit sample period (frame); otherwise it is low. MSO follows MSI by 63 transmit modulator clock (TMCLK) periods. The MSO pulse width is automatically maintained at one TMSRC period for 64X, 128X, 256X, 512X and 1024X clock sources, based on program bits P10-P12. For a single serial device, MSO is typically not connected. However, proper operation will occur if MSO is connected to MSI of the same chip. For multiple, time-synchronized transmit modulators, MSO of the master transmit modulator is typically connected to MSI of all other (slave) modulators. MSO should never be connected to $\overline{MWI}$. MSO changes synchronous to the non-sampling edge of TMSRC and is stable on the sampling edge of TMSRC. MSO is high impedance when $\overline{RESET}$ is asserted or $\overline{TOE}$ is deasserted.

If the transmit modulator is locked to the receive demodulator (P10-P12=000, the reset state), MSO does not change synchronous to TMSRC and is not maintained at one TMSRC period. MSO will be asserted high for 8 RDCLK periods during the channel A preamble of each transmit sample period (frame); otherwise it is low. MSO changes synchronous to the rising edges of the internal "RDCLK ÷ 8" clock; this "RDCLK ÷ 8" clock may be chosen as the output of the PRC and PTC pins. This "RDCLK ÷ 8" clock and associated MSO signal may be used to synchronize other transmit modulators to the receive source frequency in multiple DSP56401 systems.

3.3 Digital Audio Demodulator Signals

3.3.1 AIN0 (Audio In 0: Active High Input)

This input receives audio sample data and non-audio information modulated according to the AES/EBU/CP340 digital audio transmission standard. If AIN0 is not selected by program bits P18-19, it is ignored.

3.3.2 AIN1 (Audio In 1: Active High Input)

This input receives audio sample data and non-audio information modulated according to the AES/EBU/CP340 digital audio transmission standard. It may also receive a master synchronization sample clock for PLL frequency multiplication. If AIN1 is not selected by program bits P18-19, it is ignored.

3.3.3 AIN2 (Audio In 2: Active High Input)

This input receives audio sample data and non-audio information modulated according to the AES/EBU/CP340 digital audio transmission standard. It may also receive a master synchronization sample clock for PLL frequency multiplication. If AIN2 is not selected by program bits P18-19, it is ignored.

3.3.4 PUP (Pump Up: Active High Output)

This output provides demodulator phase and frequency correction pulses for an external voltage controlled oscillator (VCO) while locking to an incoming digital audio stream or frame clock. PUP may be lowpass filtered to produce a slowly changing control voltage for the VCO. The polarity of PUP is determined by program bit P20. If the polarity is positive (P20=0), PUP is asserted high momentarily when the phase of the modulated data input leads the phase of the recovered demodulator

clock or when the frequency of the VCO is too low; otherwise it is high impedance. If the polarity is negative (P20=1), PUP is asserted low momentarily when the phase of the modulated data input leads the phase of the recovered demodulator clock or when the frequency of the VCO is too low; otherwise it is high impedance. PUP should never be connected directly to PDOWN.

3.3.5 PDOWN (Pump Down: Active Low Output)

This output provides demodulator phase and frequency correction pulses for an external voltage controlled oscillator (VCO) while locking to an incoming digital audio stream or frame clock. PDOWN may be lowpass filtered to produce a slowly changing control voltage for the VCO. The polarity of PDOWN is determined by program bit P20. If the polarity is positive (P20=0), PDOWN is asserted low momentarily when the phase of the modulated data input lags the phase of the recovered demodulator clock or when the frequency of the VCO is too high; otherwise it is high impedance. If the polarity is negative (P20=1), PDOWN is asserted high momentarily when the phase of the modulated data input lags the phase of the recovered demodulator clock or when the frequency of the VCO is too high; otherwise it is high impedance. PDOWN should never be connected directly to PUP.

3.3.6 LOCK (Lock Indicator: Three-State Output)

This output is asserted high when the phase locked loop is locked to the incoming digital audio signal; otherwise it is low. Lock is detected from the duty cycle of the PUP and PDOWN signals. The demodulator must be locked to the incoming digital audio signal for one complete block before LOCK is asserted. LOCK is deasserted instantly if the demodulator loses lock. Once deasserted, the LOCK pin will remain low for a minimum of one complete block period before being reasserted. LOCK is high impedance when $\overline{\text{RESET}}$ is asserted or $\overline{\text{ROE}}$ is deasserted.

3.4 Receive Serial Interface Signals

3.4.1 RC (Receive Clock: Active High Input)

This input is the receive serial interface bit clock. RC may be asynchronous to TC and OSCIN0-3. However, some applications require RC to be synchronized with other clocks. At least 32 RC clocks per frame sync are required for proper operation.

3.4.2 RCP (Receive Clock Polarity: Active High Input)

This input is exclusive ORed with RC to generate the internal receive serial bit clock. If RCP is low, the RC clock input is unchanged. If RCP is high, the RC clock input is inverted. The sampling edge of RC is the falling edge if RCP=0 and is the rising edge if RCP=1. RCP should normally be hard-wired low or high for a particular application.

3.4.3 RD0 (Receive Data 0: Three-State Output)

This output supplies serial data each receive sample period (frame). RD0 is high impedance until RSI is asserted, becoming an active output synchronous to the next non-sampling edge of RC. RD0 remains active until RSO is asserted, becoming high impedance synchronous to the next non-sampling edge of RC. The number of serial bits and their order in each frame are defined by the serial mode pins M0-M2. RD0 changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC. RD0 is high impedance when $\overline{\text{RESET}}$ is asserted.

3.4.4 RD1 (Receive Data 1: Three-State Output)

This output supplies serial data each receive sample period (frame). RD1 is high impedance until RSI is asserted, becoming an active output

synchronous to the next non-sampling edge of RC. RD1 remains active until RSO is asserted, becoming high impedance synchronous to the next non-sampling edge of RC. The number of serial bits and their order in each frame are defined by the serial mode pins M0-M2. RD1 changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC. RD1 is high impedance when $\overline{\text{RESET}}$ is asserted.

3.4.5 RD2 (Receive Data 2: Three-State Output)

This output supplies serial non-audio data each receive sample period (frame). RD2 is high impedance until RSI is asserted, becoming an active output synchronous to the next non-sampling edge of RC. RD2 remains active until RSO is asserted, becoming high impedance synchronous to the next non-sampling edge of RC. The number of serial bits, bit rate and bit order in each frame are defined by the serial mode pins M0-M2. In the "fast" non-audio data modes (modes 0, 2, 4 and 6), the RD2 bit rate is equal to the RC clock rate. In the "slow" non-audio data modes (modes 1, 3, 5 and 7), the RD2 bit rate is equal to the RNS clock rate. RD2 changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC. RD2 is high impedance when $\overline{\text{RESET}}$ is asserted.

3.4.6 RBS (Receive Block Sync: Three-State Output)

This output is asserted high during the last frame period of each receive block period; otherwise it is low. The first receive data frame in the block appears on the receive data pins in the frame period following RBS high, thus RBS is an end of block indicator. RBS is derived by sampling the demodulator preamble detection and synchronizing the event to RC. RBS changes synchronous to the non-sampling edge of RC during the same RC period that RFS goes low and is stable on the sampling edge of RC. If RC is not synchronous to the receive demodulator clock, RBS may jitter due to asynchronous sampling. For jitter-free RBS operation, both RC and the receive demodulator should be driven by a common clock. This requirement can be met by driving RC from PTC or PRC programmed as a receive demodulator clock output. RBS is high impedance when $\overline{\text{RESET}}$ is asserted or $\overline{\text{ROE}}$ is deasserted.

3.4.7 RFS (Receive Frame Sync: Three-State Output)

This output is asserted high during the last RC period of each receive sample period (frame); otherwise it is low. The first receive data bit in the subframe appears on the receive data pins in the bit period following RFS high. RFS is derived by sampling the demodulator preamble detection and synchronizing the event to RC. RFS changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC. If RC is not synchronous to the receive demodulator clock, RFS may jitter due to asynchronous sampling. For jitter-free RFS operation, both RC and the receive demodulator should be driven by a common clock. This requirement can be met by driving RC from PTC or PRC programmed as a receive demodulator clock output. RFS is high impedance when $\overline{\text{RESET}}$ is asserted or $\overline{\text{ROE}}$ is deasserted.

3.4.8 RWS0 (Receive Word Sync 0: Three-State Output)

This output is asserted low each receive sample period (frame) to indicate the first bit of the channel A audio sample and is deasserted high each receive sample period to indicate the first bit of the channel B audio sample. RWS0 is asserted low in the same RC clock period that RFS is asserted and is deasserted high a fixed number of RC clock periods after RSI is asserted as defined by the serial mode pins M0-M2. See Table 3-4 for more information. If RFS is connected to RSI, the first data bit of each audio sample is output one RC clock period after RWS0 changes. RWS0 is derived by sampling the demodulator preamble detection and synchronizing the event to RC. RWS0 changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC. If RC is not synchronous to the receive demodulator clock, RWS0 may jitter due to asynchronous sampling. For jitter-free RWS0 operation, both RC and the

receive demodulator should be driven by a common clock. This requirement can be met by driving RC from PRC or PTC programmed as a receive demodulator clock output. RWS0 is high impedance when $\overline{\text{RESET}}$ is asserted or $\overline{\text{ROE}}$ is deasserted.

For stereo applications, RWS0 is a left/right channel indicator according to the I^2S convention. It may be directly used as a word select output when the DSP56401 is used as an I^2S master transmitter.

Table 3-4 RSI toRWS0 Delay

Serial Mode	Delay from RSI Assertion to RWS0 Deassertion (High)
0	24RC
1	24RC
2	32RC
3	24RC
4	16RC
5	16RC
6	24RC
7	16RC

3.4.9 RWS1 (Receive Word Sync 1: Three-State Output)

This output is asserted high each receive sample period (frame) to indicate the first bit of the channel A audio sample and is deasserted low each receive sample period to indicate the first bit of the channel B audio sample. RWS1 is asserted high in the same RC clock period that RFS is deasserted and is deasserted low a fixed number of RC clock periods after RSI is asserted as defined by the serial mode pins M0-M2. See Table 3-5 for more information. If RFS is connected to RSI, the first data bit of each audio sample is output during the same RC clock period that RWS1 changes. RWS1 is derived by sampling the demodulator preamble detection and synchronizing the event to RC. RWS1 changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC. If RC is not synchronous to the receive demodulator clock, RWS1 may jitter due to asynchronous sampling. For jitter-free RWS1 operation, both RC and the receive demodulator should be driven by a common clock. This requirement can be met by driving RC from PRC or PTC programmed as a receive demodulator clock output. RWS1 is high impedance when $\overline{\text{RESET}}$ is asserted or $\overline{\text{ROE}}$ is deasserted.

For stereo applications, RWS1 is a left/right channel indicator according to the Burr-Brown and Japanese conventions. It is derived from RWS0 inverted and delayed by one RC clock period.

Table 3-5 RSI toRWS1 Delay

Serial Mode	Delay from RSI Assertion to RWS1 Deassertion (Low)
0	25RC
1	25RC
2	33RC
3	25RC
4	17RC
5	17RC
6	25RC
7	17RC

3.4.10 RNS (Receive Non-Audio Sync: Three-State Output).

RNS is a gated clock output used to transfer non-audio data at a slower rate than its associated audio sample data. Non-audio data consists of eight bits (one byte) per sample period (frame). RNS is high impedance until RSI is asserted, becoming active synchronous to the next non-sampling edge of RC. RNS remains active until RSO is asserted, becoming high impedance synchronous to the next non-sampling edge of RC. Since RNS is high impedance during inactive time slots, an external pullup resistor is required in the system. RNS consists of eight active low clock pulses per frame, each pulse having a width of one or two RC clocks and a clock period of two or four RC clocks, depending on the serial mode. The first RNS pulse is delayed a varying number of RC

clocks after RSI is asserted, depending on the serial mode. The last RNS pulse ends ten RC clocks before RSO is asserted, independent of the serial mode. RNS changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC. See Table 3-6 and Figure 6-10 for more information. RNS may be used to directly interface non-audio data to a DSP56000 family SCI in shift register mode, a 6805 or 68HC11 SPI, or a serial-to-parallel converter. RNS is high impedance when $\overline{\text{RESET}}$ is asserted.

3.4.11 RSI (Receive Sync In: Active High Input)

This input is asserted high for one RC period of each receive sample period (frame) to begin receive data transfer; otherwise it is low. The first receive data bit is output one RC bit period after RSI is asserted. For a single serial device, RSI is typically connected to RFS. For multiple, time-multiplexed serial devices, RSI and RSO form a daisy-chain which defines receive data time slots for each serial device. In a receive daisy-chain, RSI of the first device in the chain is typically connected to RFS of the master receive device. The RSI of any other device is connected to RSO of the device occupying the previous time slot. If RSI is asserted before RSO is asserted, the current data transfer is truncated and a new data transfer is started. RSI must meet setup and hold times synchronous to the sampling edge of RC, and typically changes on the non-sampling edge of RC

3.4.12 RSO (Receive Sync Out: Active High Output)

RSO is asserted high for one RC period in each receive sample period (frame); otherwise it is low. RSO follows RSI by a fixed number of RC clock periods defined by the serial mode pins M0-M2. See Table 3-7 for more information. For a single serial device, RSO is typically not connected. For multiple, time-multiplexed serial devices, RSI and RSO form a daisy-chain which defines receive data time slots for each serial device. In a receive daisy-chain, RSO is typically connected to RSI of the serial device occupying the following receive time slot(s). RSO changes synchronous to the non-sampling edge of RC and is stable on the sampling edge of RC.

3.5 Clock Generation and Control Signals

3.5.1 OSCIN0 (Oscillator Input 0: Active High Input)

This is the input to an on-chip oscillator inverter whose output is OSCOUT0. A crystal or LC oscillator may be built using a few external components - resistors, capacitors, quartz crystal or inductor. A voltage controlled oscillator (VCO) may be designed by using external voltage controlled

Table 3-6 RNS Parameters

Serial Mode	RNS Period	RNS Width	Relative to RSI		
			RNS Begins	RNS End	RNS Driven
0	4RC	2RC	32RC	62RC	1-72RC
1	4RC	2RC	8RC	38RC	1-48RC
2	4RC	2RC	24RC	54RC	1-64RC
3	2RC	RC	7RC	22RC	1-32RC
4	4RC	2RC	8RC	38RC	1-48RC
5	2RC	RC	7RC	22RC	1-32RC
6	4RC	2RC	8RC	38RC	1-48RC
7	2RC	RC	7RC	22RC	1-32RC

Table 3-7 RSI to RSO

Serial Mode	Delay from RSI Assertion to RSO Assertion
0	72RC
1	48RC
2	64RC
3	32RC
4	48RC
5	32RC
6	48RC
7	32RC

capacitors (varactors) as part of the reactive elements of the VCO. These circuits provide a low phase jitter clock suitable for use as a Sigma-Delta data converter input clock. If an external clock source is used, it should be connected to OSCIN0. If oscillator 0 is not used, OSCIN0 should be hard-wired low. OSCIN0 is not affected by reset.

3.5.2 OSCOUT0 (Oscillator Output 0: Active High Output)

This is the output of an on-chip oscillator inverter whose input is OSCIN0. If an external clock source is connected to OSCIN0 or oscillator 0 is not used, OSCOUT0 should not be connected. OSCOUT0 should not be used to drive external loads. OSCOUT0 is not affected by reset.

3.5.3 OSCIN1 (Oscillator Input 1: Active High Input)

This is the input to an on-chip oscillator inverter whose output is OSCOUT1. A crystal or LC oscillator may be built using a few external components - resistors, capacitors, quartz crystal or inductor. A voltage controlled oscillator (VCO) may be designed by using external voltage controlled capacitors (varactors) as part of the reactive elements of the VCO.These circuits provide a low phase jitter clock suitable for use as a Sigma-Delta data converter input clock. If an external clock source is used, it should be connected to OSCIN1. If oscillator 1 is not used, OSCIN1 should be hard-wired low. OSCIN1 is not affected by reset.

3.5.4 OSCOUT1 (Oscillator Output 1: Active High Output)

This is the output of an on-chip oscillator inverter whose input is OSCIN1. If an external clock source is connected to OSCIN1 or oscillator 1 is not used, OSCOUT1 should not be connected. OSCOUT1 should not be used to drive external loads. OSCOUT1 is not affected by reset.

3.5.5 OSCIN2 (Oscillator Input 2: Active High Input)

This is the input to an on-chip oscillator inverter whose output is OSCOUT2. A crystal or LC oscillator may be built using a few external components - resistors, capacitors, quartz crystal or inductor. A voltage controlled oscillator (VCO) may be designed by using external voltage controlled capacitors (varactors) as part of the reactive elements of the VCO. These circuits provide a low phase jitter clock suitable for use as a Sigma-Delta data converter input clock. If an external clock source is used, it should be connected to OSCIN2. If oscillator 2 is not used, OSCIN2 should be hard-wired low. OSCIN2 is not affected by reset.

3.5.6 OSCOUT2 (Oscillator Output 2: Active High Output)

This is the output of an on-chip oscillator inverter whose input is OSCIN2. If an external clock source is connected to OSCIN2 or oscillator 2 is not used, OSCOUT2 should not be connected. OSCOUT2 should not be used to drive external loads. OSCOUT2 is not affected by reset.

3.5.7 OSCIN3 (Oscillator Input 3: Active High Input)

This is the input to an on-chip oscillator inverter whose output is OSCOUT3. A crystal or LC oscillator may be built using a few external components - resistors, capacitors, quartz crystal or inductor. A voltage controlled oscillator (VCO) may be designed by using external voltage controlled capacitors (varactors) as part of the reactive elements of the VCO. These circuits provide a low

phase jitter clock suitable for use as a Sigma-Delta data converter input clock. If an external clock source is used, it should be connected to OSCIN3. If oscillator 3 is not used, OSCIN3 should be hard-wired low. OSCIN3 is not affected by reset.

3.5.8 OSCOUT3 (Oscillator Output 3: Active High Output)

This is the output of an on-chip oscillator inverter whose input is OSCIN3. If an external clock source is connected to OSCIN3 or oscillator 3 is not used, OSCOUT3 should not be connected. OSCOUT3 should not be used to drive external loads. OSCOUT3 is not affected by reset.

3.5.9 PTC (Programmable Transmit Clock: Active High Output)

This output provides a programmable system clock which may be used as a serial interface bit clock or as a Sigma-Delta data converter input clock. Any on-chip oscillator may be selected as the clock source, whose frequency may be modified by an on-chip programmable clock generator. When PTC is sourced from a divided-down TMSRC, that clock is phase adjusted by MSI or $\overline{\text{MWI}}$ to automatically align its rising edge with the TMSRC rising edge that follows the MSI or $\overline{\text{MWI}}$ assertion. Since divided down versions of TMSRC are phase adjusted by MSI or $\overline{\text{MWI}}$, the transmit divider chain (via the PTC output - refer to Figure 2-7) should not be used to generate the MSI or $\overline{\text{MWI}}$ inputs or erratic operation will result. PTC is controlled by the program word which is described in Section 4.2. PTC is high impedance when $\overline{\text{TOE}}$ is deasserted.

3.5.10 PRC (Programmable Receive Clock: Active High Output)

This output provides a programmable system clock which may be used as a serial interface bit clock or as a Sigma-Delta data converter input clock. Any on-chip oscillator may be selected as the clock source, whose frequency may be modified by an on-chip programmable clock generator. PRC is controlled by the program word which is described in Section 4.2. PRC is high impedance when $\overline{\text{ROE}}$ is deasserted.

3.5.11 $\overline{\text{PRGE}}$ (Program Enable: Active Low Input)

This input is asserted low to enable the transmit serial interface to shift in and load program bits. If $\overline{\text{PRGE}}$ is deasserted high, then the transmit serial interface will not load new program bits or latch in a new program word, regardless of the state of the channel A and B parity bits (refer to Section 5.2.7). $\overline{\text{PRGE}}$ may be asserted and deasserted synchronous or asynchronous with the shifting in of data bits. A proper program word load sequence will then transmit 24 contiguous frames with Ap=1 followed by at least one frame with Ap=0.

The usual method is to assert and deassert $\overline{\text{PRGE}}$ asynchronous to the bit shifting. $\overline{\text{PRGE}}$ must be asserted low prior to the beginning of the first frame in which the user sets Ap to 1with the intention of shifting in program bits. $\overline{\text{PRGE}}$ should not be deasserted high again until **after** the second frame with Ap=0.

If the user elects to assert and deassert the $\overline{\text{PRGE}}$ synchronously, $\overline{\text{PRGE}}$ must be asserted low at least three TC sampling edges before the TSO assertion associated with the first frame in which the user sets Ap to 1 with the intention of shifting in program bits and deasserted high no sooner than 2 TC clock periods after the end of the time slot. This sequence is repeated for each of the following 25 frames (26 total: 24 with Ap=1 followed by 2 with Ap=0). $\overline{\text{PRGE}}$ should not be deasserted and left high until after the second frame with Ap=0.

$\overline{\text{PRGE}}$ is provided as additional protection for systems which cannot ensure that Ap will always equal 0 when not shifting in program bits and is often useful while debugging the application interface code. Final systems which can ensure proper control of the Ap bit at all times may have the $\overline{\text{PRGE}}$ pin permanently asserted low.

3.5.12 PS0 (Program/Status 0: Open Drain, Input/Output)

As an input, the PS0 logic level is available as status bit S0. An external pullup resistor is required to achieve a high logic level. S0 directly samples the

PS0 pin once per block when the Frame 184 Ac (Channel A Channel Status) bit is sampled by the receive demodulator. As an output, PS0 is asserted low when the program word bit P0 is set; otherwise it is high impedance. PS0 changes one-half TC clock after TSO is deasserted if the program register is parallel loaded during the current frame. Due to the serial protocol, PS0 cannot change more than once every 25 frames. PS0 may be used to gate oscillators on/off, switch VCO frequency ranges or as a general-purpose I/O pin. PS0 is high impedance when $\overline{\text{RESET}}$ is asserted.

3.5.13 PS1 (Program/Status 1: Open Drain, Input/Output)

As an input, the PS1 logic level is available as status bit S1. An external pullup resistor is required to achieve a high logic level. S1 directly samples the PS1 pin once per block when the Frame 184 Bc (Channel B Channel Status) bit is sampled by the receive demodulator. As an output, PS1 is asserted low when the program word bit P1 is set; otherwise it is high impedance. PS1 changes one-half TC clock after TSO is deasserted if the program register is parallel loaded during the current frame. Due to the serial protocol, PS1 cannot change more than once every 25 frames. PS1 may be used to gate oscillators on/off, switch VCO frequency ranges or as a general-purpose I/O pin. PS1 is high impedance when $\overline{\text{RESET}}$ is asserted.

3.5.14 PS2 (Program/Status 2: Open Drain, Input/Output)

As an input, the PS2 logic level is available as status bit S2. An external pullup resistor is required to achieve a high logic level. S2 directly samples the PS2 pin once per block when the Frame 185 Ac (Channel A Channel Status) bit is sampled by the receive demodulator. As an output, PS2 is asserted low when the program word bit P2 is set; otherwise it is high impedance. PS2 changes one-half TC clock after TSO is deasserted if the program register is parallel loaded during the current frame. Due to the serial protocol, PS2 cannot change more than once every 25 frames. PS2 may be used to gate oscillators on/off, switch VCO frequency ranges or as a general-purpose I/O pin. PS2 is high impedance when $\overline{\text{RESET}}$ is asserted.

3.5.15 PS3 (Program/Status 3: Open Drain, Input/Output)

As an input, the PS3 logic level is available as status bit S3. An external pullup resistor is required to achieve a high logic level. S3 directly samples the PS3 pin once per block when the Frame 185 Bc (Channel B Channel Status) bit is sampled by the receive demodulator. As an output, PS3 is asserted low when the program word bit P3 is set; otherwise it is high impedance. PS3 changes one-half TC clock after TSO is deasserted if the program register is parallel loaded during the current frame. Due to the serial protocol, PS3 cannot change more than once every 25 frames. PS3 may be used to gate oscillators on/off, switch VCO frequency ranges or as a general-purpose I/O pin. PS3 is high impedance when $\overline{\text{RESET}}$ is asserted.

3.5.16 $\overline{\text{TOE}}$ (Transmit Output Enable, Active Low Input)

This input is asserted low to enable the TBS and TFS outputs of the transmit serial interface, the MSO output of the transmit modulator and the PTC output of the clock generator; otherwise they are high impedance. For a single serial device, $\overline{\text{TOE}}$ is always asserted low. For multiple DSP56401 systems, $\overline{\text{TOE}}$ is asserted low to select which serial device provides the master transmit bit clock, frame sync and block sync signals to other modulators and serial devices. If multiple DSP56401 devices share one SSI or SCI port, only one $\overline{\text{TOE}}$ may be asserted at a time.

3.5.17 $\overline{\text{ROE}}$ (Receive Output Enable, Active Low Input)

This input is asserted low to enable the RBS, RFS, RWS0 and RWS1 outputs of the receive serial interface, the LOCK output of the receive demodulator and the PRC output of the clock generator; otherwise they are high impedance. For a single serial device, $\overline{\text{ROE}}$ is always asserted low. For multiple DSP56401 systems, $\overline{\text{ROE}}$ is asserted low to select which serial device provides the master receive bit clock, frame sync and block sync

signals to other demodulators and serial devices. If multiple DSP56401 devices share one SSI or SCI port, only one $\overline{ROE}$ may be asserted at a time.

3.5.18 M0, M1 and M2 (Serial Mode 0, 1 and 2: Active High Inputs)

These inputs select the serial mode for the transmit and receive serial interfaces. The serial mode defines the usage of each serial interface data pin and the number of serial bits, bit rate and bit ordering of serial data transfers. M0-M2 are generally hard-wired low or high in a given application but may be controlled by a programmable I/O pin on a host DSP. Section 5 describes the details of each serial mode.

Table 3-8 Serial Modes

Serial Mode Pins			
M2	M1	M0	Serial Mode
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

3.5.19 $\overline{RESET}$ (Reset: Active Low Input)

This input is asserted low to reset internal circuits after powerup. $\overline{RESET}$ may be asserted low or deasserted high asynchronously. $\overline{RESET}$ is typically tied to a DSP $\overline{RESET}$ line or controlled by a programmable I/O pin on a host DSP.

3.5.20 VDDI (Internal Logic Power: 2 pins)

These power supply pins connect the internal logic circuits to an external +5 volt DC supply. High frequency decoupling capacitors should be connected as closely as possible to each pair of VDDI/VSSI pins.

3.5.21 VSSI (Internal Logic Ground: 4 pins)

These power supply pins connect the internal logic circuits to an external ground. High frequency decoupling capacitors should be connected as closely as possible to each pair of VDDI/VSSI pins.

3.5.22 VDDB (Output Buffer Power: 3 pins)

These power supply pins connect the internal output buffer circuits to an external +5 volt DC supply. High frequency decoupling capacitors should be connected as closely as possible to each pair of VDDB/VSSB pins.

3.5.23 VSSB (Output Buffer Ground: 4 pins)

These power supply pins connect the internal output buffer circuits to an external ground. High frequency decoupling capacitors should be connected as closely as possible to each pair of VDDB/VSSB pins.

Program and Status Word

4.1 General overview

Many on-chip options are controlled by a 24-bit program word (bits P0-P23) loaded through the transmit serial interface. On-chip status information is available in a 16-bit status word (bits S0-S15) sent out through the receive serial interface. Both the program word and the status word are subsets of the non-audio data, utilizing either the parity bit (host DSP to transmit serial interface) or the channel status bit (receive serial interface to host DSP). The serial format, including pin usage and shift clock frequency, is defined by the serial mode pins M0-M2, as described in Sections 3.5.18, 5.1 and 5.2.

Since the DSP56401 generates parity information in hardware, it does not need to communicate parity bits from the host DSP to the DSP56401, leaving these bits available for programming the DSP56401. When the Channel A parity bit equals one, the Channel B parity bit is shifted into the temporary program word shift register. The 24-bit program word is shifted in, one bit at a time, over 24 consecutive digital audio frames. When the Channel A parity bit returns low after having been high for more than one frame, the received word in the temporary program word shift register is loaded into the program word register and selects the appropriate options for DSP56401 operation. This program word is defined below, in Section 4.2. See Figure 5-2 and Section 5.2.7 for more information on loading the program word.

The AES and EBU standards, along with the CP340 professional standard, use the last eight bits of the channel status block of each channel for Cyclic Redundancy Checking (CRC), with each channel checked separately. Since the DSP56401 verifies the CRC in hardware, it can collapse the eight bits of Channel A CRC and the eight bits of Channel B CRC into two bits, Channel A CRC error (S14) and Channel B CRC error (S15). This leaves fourteen Channel Status bits per block of 192 digital audio frames available for communicating DSP56401 operational status information to the host DSP, as well as freeing the host DSP from the CRC verification overhead. These operational status bits are shifted out, two bits per each non-audio data word, in the last eight non-audio data words of the 192-frame block. This status word is defined below, in Section 4.3. See Figure 5-5 and Sections 5.4.5 and 5.4.6 for more information on receiving the status word.

4.2 Program Word Definition

The program bits P0-P23 are defined below. There is also a program word worksheet in Appendix C to aid in formulating a program word. $\overline{\text{PRGE}}$ must be asserted low to program the DSP56401 prior to the beginning of the first frame in which the user sets Ap to 1, and may optionally be deasserted high to "lock in" the program word two or more frames after Ap returns to 0 following two or more frames where Ap was 1. During loading, program bit 0 is shifted in first and program bit 23 is shifted in last. All program bits are asynchronously cleared to a "reset" state when $\overline{\text{RESET}}$ is asserted low.

4.2.1 P0, P1, P2, P3 (Programmable Outputs 0, 1, 2, 3)

These bits control open-drain output drivers on pins PS0, PS1, PS2 and PS3, respectively. Since these pins are active low, an external pullup resistor is required for a high logic level.

Pn	Programmable Output (where n = 0, 1, 2, 3)
0	PSn is high impedance (reset state).
1	PSn is asserted low.

4.2.2 P4, P5 (Receive Demodulator Clock Source)

These bits select the external clock source (RDSRC) for the receive demodulator clock generator.

P5	P4	Receive Demodulator Source (RDSRC)
0	0	OSCIN0 (reset state).
0	1	OSCIN1.
1	0	OSCIN2.
1	1	OSCIN3.

4.2.3 P6, P7 (Receive Demodulator Clock Generator)

These bits select the receive demodulator clock (RDCLK) frequency. They control the divide ratio between RDSRC and RDCLK. RDCLK is always 512 times the receive demodulator sample rate. When RDSRC is multiplied by 2 or divided by 1.5, the RDCLK duty cycle depends on the RDSRC duty cycle which should be nominally 50 percent. For other divide ratios, the duty cycle is not important.

P7	P6	Receive Demodulator Clock (RDCLK)
0	0	RDSRC ÷ 2 (reset state). RDSRC is 1024 times the sample rate.
0	1	RDSRC x 2 (internal clock frequency doubler). RDSRC is 256 times the sample rate.
1	0	RDSRC ÷ 1.5. RDSRC is 768 times the sample rate.
1	1	RDSRC ÷ 1. RDSRC is 512 times the sample rate.

4.2.4 P8, P9 (Transmit Modulator Clock Source)

These bits select the external clock source (TMSRC) for the transmit modulator clock generator. This clock source selection may be overruled by P10-P12.

P9	P8	Transmit Modulator Source (TMSRC)
0	0	TC (reset state).
0	1	OSCIN1.
1	0	OSCIN2.
1	1	OSCIN3.

4.2.5 P10, P11, P12 (Transmit Modulator Clock Generator)

These bits select the transmit modulator clock (TMCLK) frequency. They select either the demodulator clock or TMSRC for a source. If TMSRC is selected, P10, P11, and P12 control the divide ratio between TMSRC and TMCLK. TMCLK is always 64 times the transmit modulator sample rate. When TMSRC is divided by 1, the TMSRC duty cycle should be nominally 50 percent. For other divide ratios, the duty cycle is not important.

P12	P11	P10	Transmit Modulator Clock (TMCLK)
0	0	0	Lock to demodulator clock and demodulator frame sync (reset state).
0	0	1	TMSRC ÷ 2. TMSRC is 128 times the sample rate. TMCLK is phase adjusted by MSI or $\overline{\text{MWI}}$.
0	1	0	TMSRC ÷ 4. TMSRC is 256 times the sample rate. TMCLK is phase adjusted by MSI or $\overline{\text{MWI}}$.
0	1	1	TMSRC ÷ 8. TMSRC is 512 times the sample rate. TMCLK is phase adjusted by MSI or $\overline{\text{MWI}}$.
1	0	0	TMSRC ÷ 16. TMSRC is 1024 times the sample rate. TMCLK is phase adjusted by MSI or $\overline{\text{MWI}}$.
1	0	1	Reserved.
1	1	0	TMSRC ÷ 1. TMSRC is 64 times the sample rate.
1	1	1	Reserved.

4.2.6 P13, P14, P15 (Programmable Transmit Clock Source)

These bits select the output clock present on the PTC pin. PTC is high impedance if $\overline{\text{TOE}}$ is deasserted. When TMSRC is divided by 1, the PTC duty cycle depends on the TMSRC duty cycle. For other divide ratios, the PTC duty cycle is nominally 50 percent.

P15	P14	P13	Programmable Transmit Clock (PTC)
0	0	0	RDCLK ÷ 4 (reset state). PTC is 128 times the transmit or receive sample rate.
0	0	1	RDCLK ÷ 8. PTC is 64 times the transmit or receive sample rate.
0	1	0	RDCLK ÷ 2. PTC is 256 times the transmit or receive sample rate.
0	1	1	TMCLK ÷ 64. PTC is phase adjusted by MSI or $\overline{\text{MWI}}$ except when the transmit modulator is locked to the receive demodulator. PTC is the transmit sample rate.
1	0	0	TMSRC ÷ 8. PTC is phase adjusted by MSI or $\overline{\text{MWI}}$.
1	0	1	TMSRC ÷ 4. PTC is phase adjusted by MSI or $\overline{\text{MWI}}$.
1	1	0	TMSRC ÷ 2. PTC is phase adjusted by MSI or $\overline{\text{MWI}}$.
1	1	1	TMSRC ÷ 1.

4.2.7 P16, P17 (Programmable Receive Clock Source)

These bits select the output clock present on the PRC pin. PRC is high impedance if $\overline{ROE}$ is deasserted. When RDCLK is divided by 1, the PRC duty cycle depends on the RDCLK duty cycle. For other divide ratios, the PRC duty cycle is nominally 50 percent.

P17	P16	Programmable Receive Clock (PRC)
0	0	RDCLK ÷ 2 (reset state). PRC is 256 times the transmit or receive sample rate.
0	1	RDCLK ÷ 4. PRC is 128 times the transmit or receive sample rate.
1	0	RDCLK ÷ 8. PRC is 64 times the transmit or receive sample rate.
1	1	RDCLK ÷ 1. PRC is 512 times the transmit or receive sample rate.

4.2.8 P18, P19 (Receive Demodulator Audio Source)

These bits select the receive demodulator audio source. If the demodulator input is set to zero, the internal state machine free-runs to create its own periodic frame and block sync signals. Note that no input is selected after powerup or reset and an input must be enabled to receive frame sync or digital audio.

P19	P18	Receive Demodulator Audio Source
0	0	Zero input (reset state).
0	1	AIN0 input pin.
1	0	AIN1 input pin.
1	1	AIN2 input pin.

4.2.9 P20 (Receive Demodulator PLL Polarity)

This bit determines the polarity of the receive demodulator phase lock loop (PLL) phase detector output pins (PUP and PDOWN). The polarity of the PUP and PDOWN pins is selected by P20. If P20 is cleared, the phase detector output polarity is positive, which usually implies a non-inverting loop filter in the VCO control circuit. If P20 is set, the phase detector output polarity is negative, which usually implies an inverting loop filter in the VCO control circuit.

P20	Phase Lock Loop Mode
0	Positive phase detector polarity (reset state).
1	Negative phase detector polarity.

4.2.10 P21 (Receive Demodulator PLL Mode)

This bit determines the function of the receive demodulator phase lock loop (PLL). The PLL may lock to a digital audio bit stream present on a selected AIN pin. This is used when the receive demodulator clock is derived locally from the digital audio transmission standard. The receive PLL may also lock to a sample clock present on a selected AIN pin. This is used when the transmit modulator clock is derived from a studio master synchronization frame (sample) clock and can enable facility-wide synchronization of digital audio. P21 selects the mode; if it is cleared, the receive PLL will lock to incoming digital audio. If P21 is set, the receive PLL will lock to incoming frame sync.

P21	Phase Lock Loop Mode
0	Lock to digital audio input (reset state).
1	Lock to frame clock (sample frequency).

4.2.11 P22 (Transmit Modulator CRC)

These bits control data transmission on the AOUT pin. The transmit channel status CRC bytes may be calculated and transmitted, or disabled, passing through the received non-audio Channel Status bits corresponding to those positions.

P22	Transmit Modulator Mode
0	CRC disabled (reset state).
1	CRC enabled.

4.2.12 P23 (Transmit Modulator Mute)

This bit controls data transmission on the AOUT pin. The transmit modulator may be muted by transmitting zero valued audio samples, ignoring any data that is received by the transmit serial interface, or it may transmit audio samples received by the transmit serial interface.

P23	Transmit Modulator Mode
0	Zero valued audio samples are transmitted (reset state).
1	Transmit serial interface audio samples.

4.3 Status Word Definition

The status bits S0-S15 are defined below. There is also a status word worksheet in Appendix C to aid in interpreting a particular status word. During readout, status bit S0 is the first bit shifted out and S15 is the last bit shifted out. The status bits are undefined when $\overline{\text{RESET}}$ is asserted.

4.3.1 S0, S1, S2, S3 (Status Inputs 0, 1, 2, 3)

These bits indicate the state of pins PS0, PS1, PS2 and PS3, respectively. For use as an input-only pin, the corresponding program bit P0, P1, P2 or P3 must be cleared.

Sn	Status Input Pin (where n = 0, 1, 2, 3)
0	Low logic level on PSn.
1	High logic level on PSn.

4.3.2 S4 (Signal Present)

This bit indicates the presence of a receive signal on the selected AIN pin. The input signal must change logic levels at least once per two frame periods to be detected as present.

S4	Meaning
0	No signal detected.
1	Signal present.

4.3.3 S5 (Receive Demodulator Lock Detect)

This bit indicates that the receive PLL is locked to a digital audio bit stream or sample clock present on a selected AIN pin. Lock is detected from the duty cycle of the PUP and PDOWN signals. The demodulator must be locked to the incoming digital audio signal for one complete block before the lock bit is set. The lock bit is cleared if the demodulator loses lock and is updated once per frame. Once deasserted, the lock bit will remain clear for a minimum of one complete block period before being set again.

4.3.4 S6 (PLL Frequency High)

This bit indicates that the PLL frequency is too high compared to the demodulator AIN input pin. This may be used to determine the input bit rate on a selected AIN pin to switch VCO frequencies to obtain PLL lock. If S6 is set, the PLL is not locked.

S5	Meaning
0	PLL not locked.
1	PLL locked.

S6	Meaning
0	PLL frequency not too high.
1	PLL frequency too high.

4.3.5 S7 (PLL Frequency Low)

This bit indicates that the PLL frequency is too low compared to the demodulator AIN input pin. This may be used to determine the input bit rate on a selected AIN pin to switch VCO frequencies to obtain PLL lock. If S7 is set, the PLL is not locked.

S7	Meaning
0	PLL frequency not too low.
1	PLL frequency too low.

4.3.6 S8-S13 (Reserved)

These bits are reserved and read as zero.

4.3.7 S14 (Channel A CRC Error)

This bit indicates that a CRC error was detected in the current channel A channel status block. This bit is undefined if the PLL mode is not locking to the digital audio transmission standard or if the PLL is not locked. If the channel A CRC was not transmitted, S14 will indicate false CRC errors.

S14	Meaning
0	No channel A CRC error.
1	Channel A CRC error.

4.3.8 S15 (Channel B CRC Error)

This bit indicates that a CRC error was detected in the current channel B channel status block. This bit is undefined if the PLL mode is not locking to the digital audio transmission standard or if the PLL is not locked. If the channel B CRC was not transmitted, S15 will indicate false CRC errors.

S15	Meaning
0	No channel B CRC error.
1	Channel B CRC error.

Serial Modes

The serial modes allow flexible interfacing in a variety of systems. The transmit and receive serial interfaces operate in one of eight modes selected by the serial mode pins M0, M1 and M2. The transmit and receive serial mode are always the same. A summary of the serial modes is shown in Figure 5-1.

Each serial mode defines the bit ordering and pin usage for transferring one frame of audio samples and non-audio data. This sequence repeats each frame, synchronized by the frame or word sync inputs. The following sections use shift registers to functionally describe each serial mode. The data in the shift registers is shifted from right to left. A DSP56000 family SSI should use its default MSB-first transfer mode for the audio samples. A DSP56000 family SCI may use its default LSB-first or its optional MSB-first transfer mode for the non-audio data.

5.1 Transmit Modes

The transmit serial interface may be viewed as one, two or three shift registers clocked by TC (or TNS for the slow non-audio data modes), whose data is loaded from TD0, TD1 or TD2. Figure 5-2Figure 5-2 illustrates the pin usage, serial bit count and bit ordering of each transmit serial mode. After the serial bit count is reached, the shift registers stop shifting until the next TSI assertion. When using modes 1, 5 and 6, there must be a minimum gap of 6 TC clocks between when the shift registers stop shifting and the next assertion of TFS output. Modes 0, 2, 3, 4 and 7 have additional reserved bits within the time slot after shifting is completed and so are not affected as long as the TSO assertion to TFS assertion specification of 0 TC clocks is met. Another way to look at this is that there must be a sufficient number of TC clocks per frame to allow TSO to be produced each frame, whether the DSP56401 is operating as a serial bus master or slave. If the DSP56401 is the sole occupant of the serial bus, mode 1 would then require a a minimum bit count per frame of 54 bits, mode 5 would require 38 bits, and mode 6 would require 54 bits. With the wide variety of clock division ratios available on the DSP56401, this is generally not a problem. If there are other devices occupying additional serial bus time slots, this requirement is satisfied and no extra bit periods need be added to the frame. Shift register fields shown as "reserved" should be written with zeroes for future compatibility.

Serial Mode	Data Size (bits)	Time Slot Size (bits)	Number of Time Slots	Non-Audio Data Rate	Typical Application
0	24	24	3	Fast	24 Bit Professional DSP56001
1	24	24	2	Slow	24 Bit Professional DSP56001, 24 Bit I^2S
2	24	16	4	Fast	24 Bit Professional DSP56156
	24	32	2	Fast	24 Bit DSP32C, TMS320C30
3	24	24	1	Slow	24 Bit A/D-D/A
4	16	16	3	Fast	16 Bit Consumer DSP56001, DSP56156
5	16	16	2	Slow	16 Bit Consumer DSP56001, DSP56156, Stereo DSP56351, 16 Bit I^2S
6	24	24	2	Fast	24 Bit Professional DSP56001, 24 Bit I^2S
7	16	16	1T,2R	Slow	Time-Sync Stereo DSP56ADC16

where T = Transmit, R = Receive, Fast = TC or RC clock rate, Slow = TNS or RNS clock rate

Figure 5-1 Serial Mode Summary

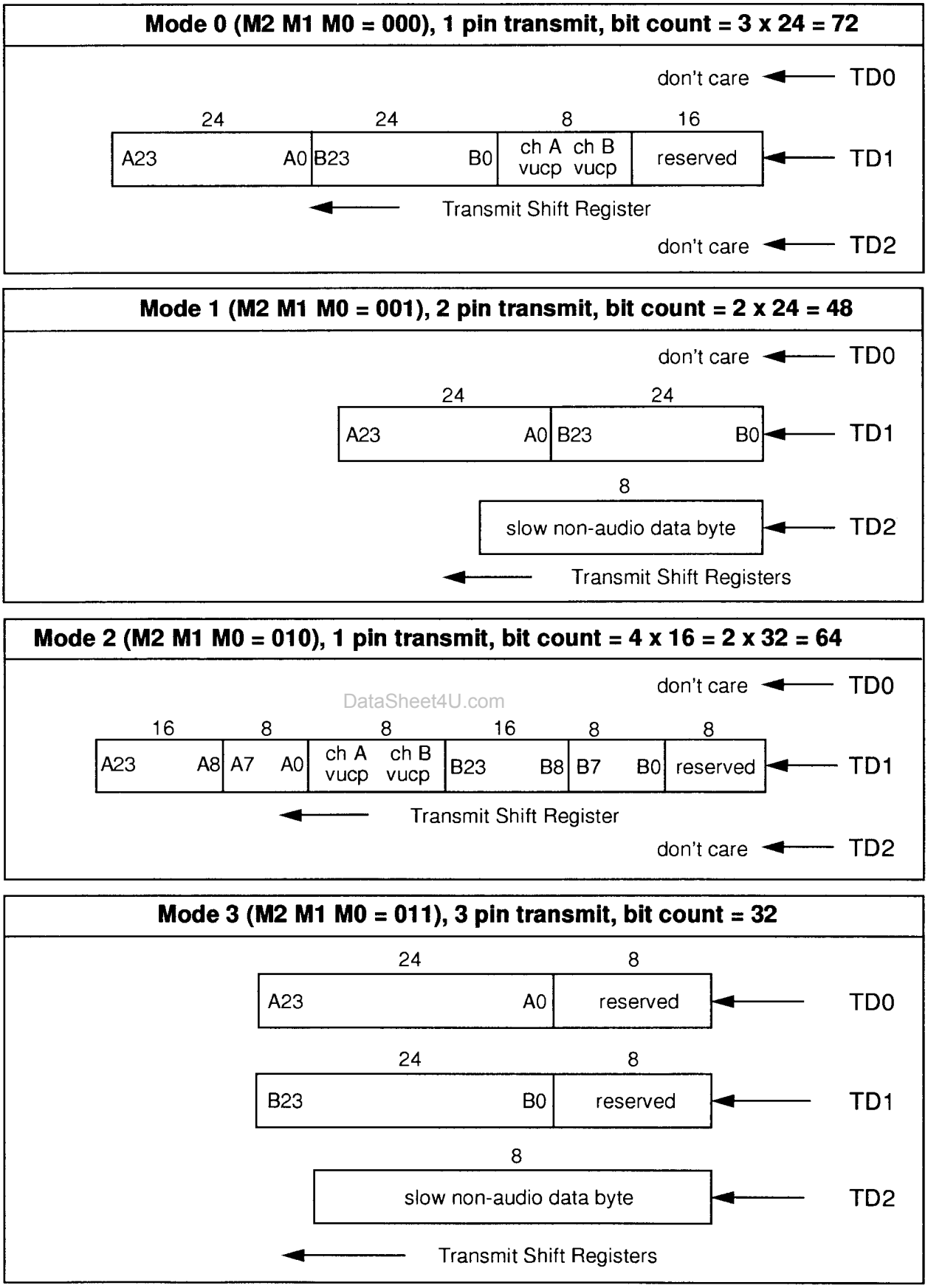


Figure 5-2 Transmit Serial Modes

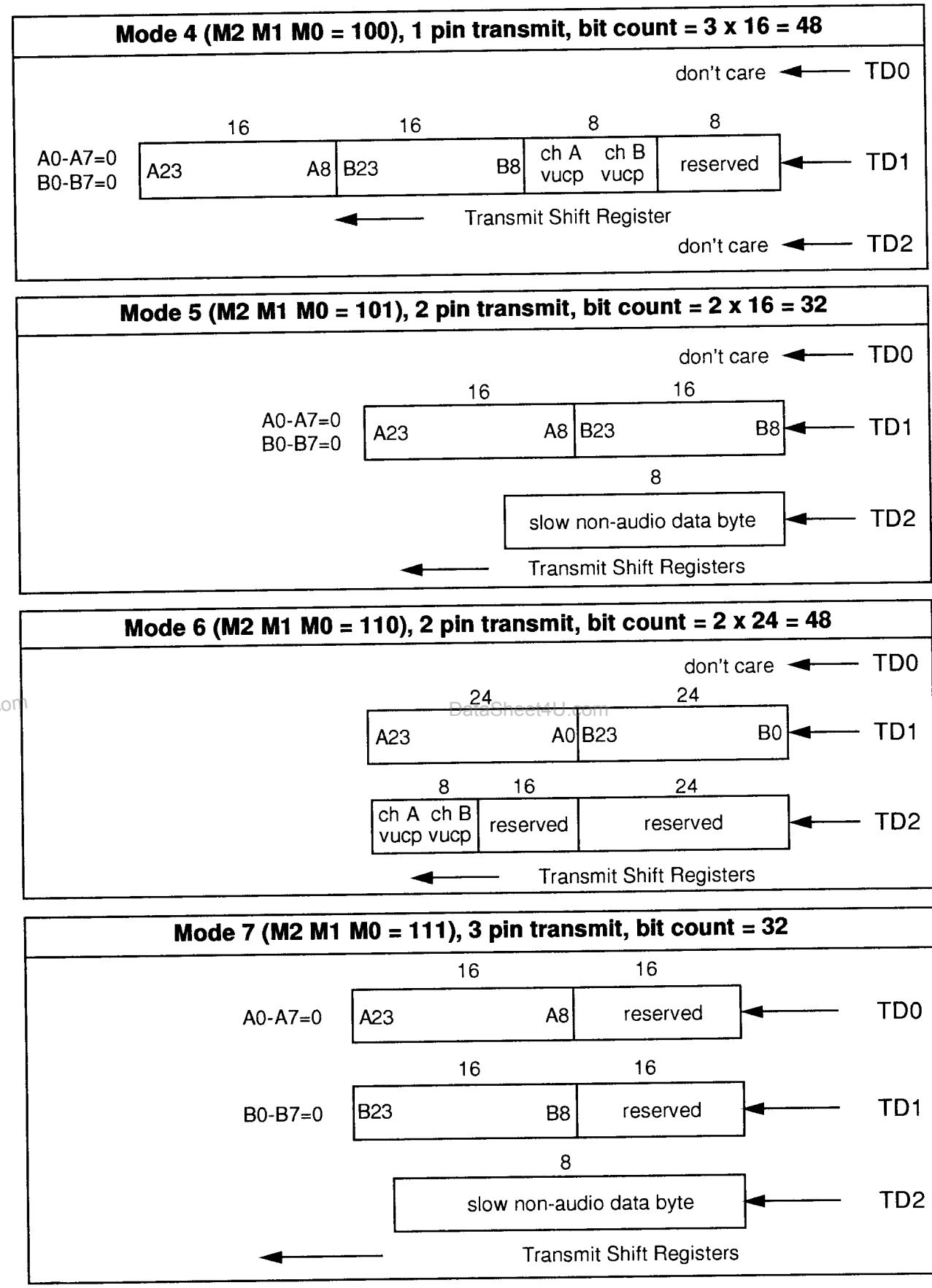


Figure 5-2 Transmit Serial Modes (continued)

5.2 Transmit Non-Audio Data Format

Transmit non-audio data consists of eight bits (one byte) per sample period (frame). Depending on the serial mode, the non-audio data may enter the DSP56401 on the same pin with audio sample data, or may enter through a separate pin. A "fast" non-audio mode (modes 0, 2, 4, 6) exists when the non-audio data is serially clocked by TC. A "slow" non-audio mode (modes 1, 3, 5, 7) exists when the non-audio data is serially clocked by TNS. Data clocked into TD1 is "fast" non-audio data and, except for serial mode 6, data clocked into TD2 is "slow" non-audio data. Regardless of the serial rate or pin used, the non-audio data byte format is always the same.

Transmit non-audio data is organized into blocks of 192 frames, numbered 0-191. The total non-audio information transferred each block is 192 bytes. The transmit block sync (TBS) signal may be examined by the user to identify the last non-audio byte in a block, or the user may define the first non-audio byte in the block by using the "force transmit block reset" command. The meaning of channel status and user bits within each non-audio data byte in a block depends on its frame number relative to the beginning of the block, as shown in Figure 5-3. Since Figure 5-3 represents physical shift registers which are loaded from right to left, the first bit entered is on the left and the last bit entered is on the right. In this section, the notation "Av" is used to indicate the "Channel A Validity" bit, and so on.

5.2.1 Channel A Validity (Av) Bit

This bit is cleared if the corresponding channel A audio sample is suitable for D/A conversion. Av is set if the corresponding channel A audio sample is unsuitable for D/A conversion. If there is no way to interpret the validity of audio samples (such as continuous audio samples directly from an A/D converter), Av should be cleared.

5.2.2 Channel B Validity (Bv) Bit

This bit is cleared if the corresponding channel B audio sample is suitable for D/A conversion. Bv is set if the corresponding channel B audio sample is unsuitable for D/A conversion. If there is no way to interpret the validity of audio samples (such as continuous audio samples directly from an A/D converter), Bv should be cleared.

5.2.3 Channel A User Data (Au) Bit

This bit is not defined by the digital audio transmission standard (it is defined within the compact disc format and in AES18-1992) and is available for user-specific features. Although block synchronization may be used, the Au bit has no restrictions on block size or serial protocol. If user data bits are not implemented, Au should be cleared.

5.2.4 Channel B User Data (Bu) Bit

This bit is not defined by the digital audio transmission standard (it is defined within the compact disc format and in AES18-1992) and is available for user-specific features. Although block synchronization may be used, the Bu bit has no restrictions on block size or serial protocol. If user data bits are not implemented, Bu should be cleared.

5.2.5 Channel A Channel Status (Ac) Bit

This bit is used to transmit the channel status bit for the channel A subframe. A block of 192 Ac bits forms the channel A channel status block defined by the digital audio transmission standard. Frame zero of the Ac bits must be synchronized with the transmit block sync (TBS) pin or by the transmit block reset command for proper alignment with the modulator preamble sync patterns.

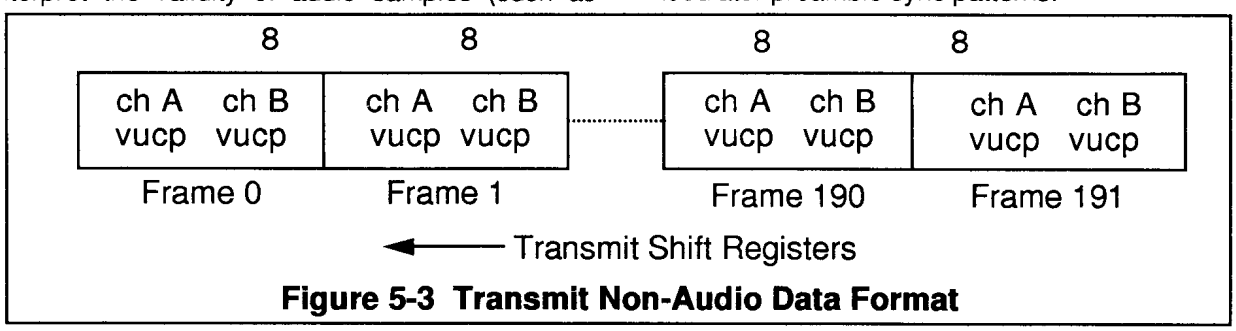


Figure 5-3 Transmit Non-Audio Data Format

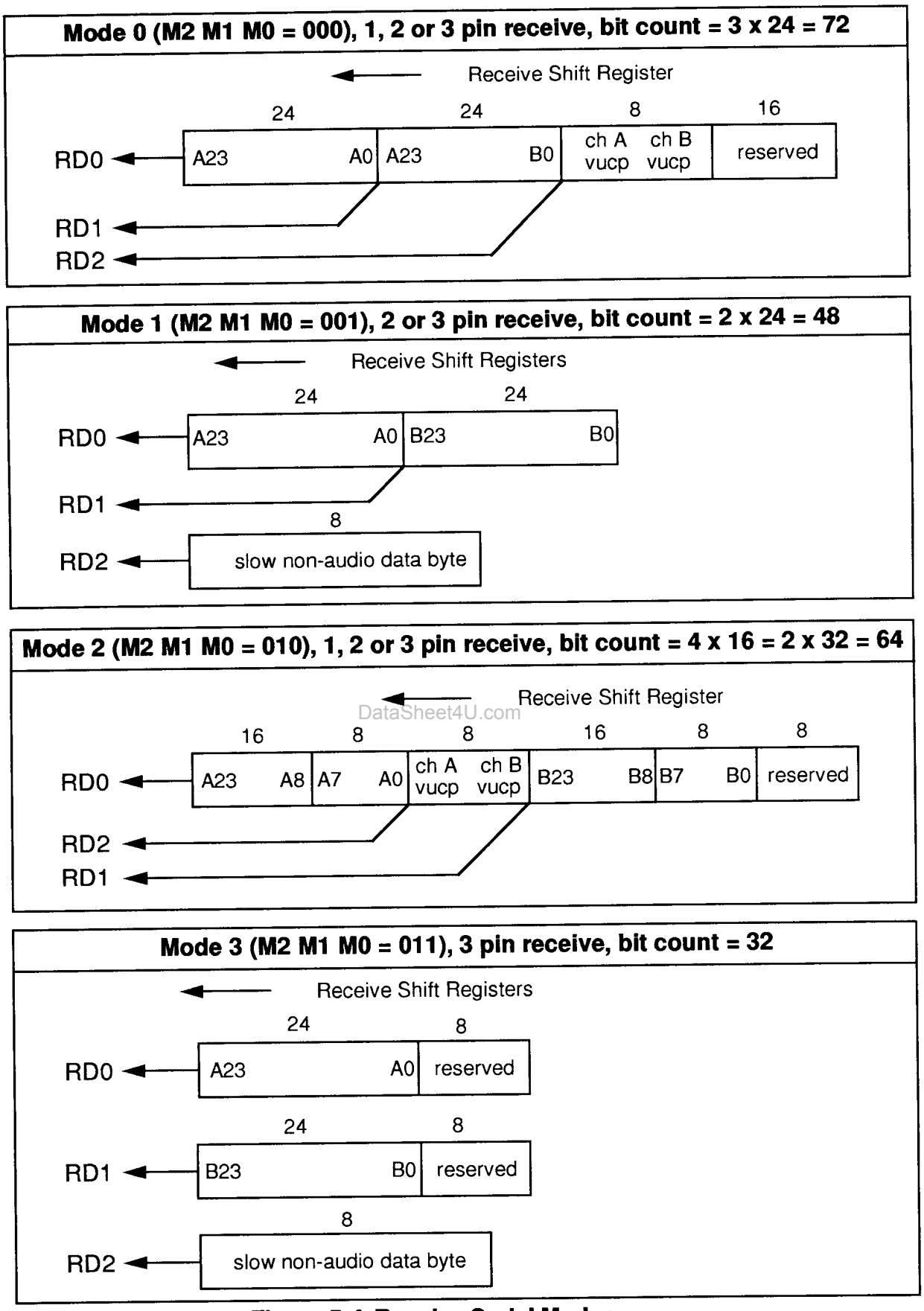


Figure 5-4 Receive Serial Modes

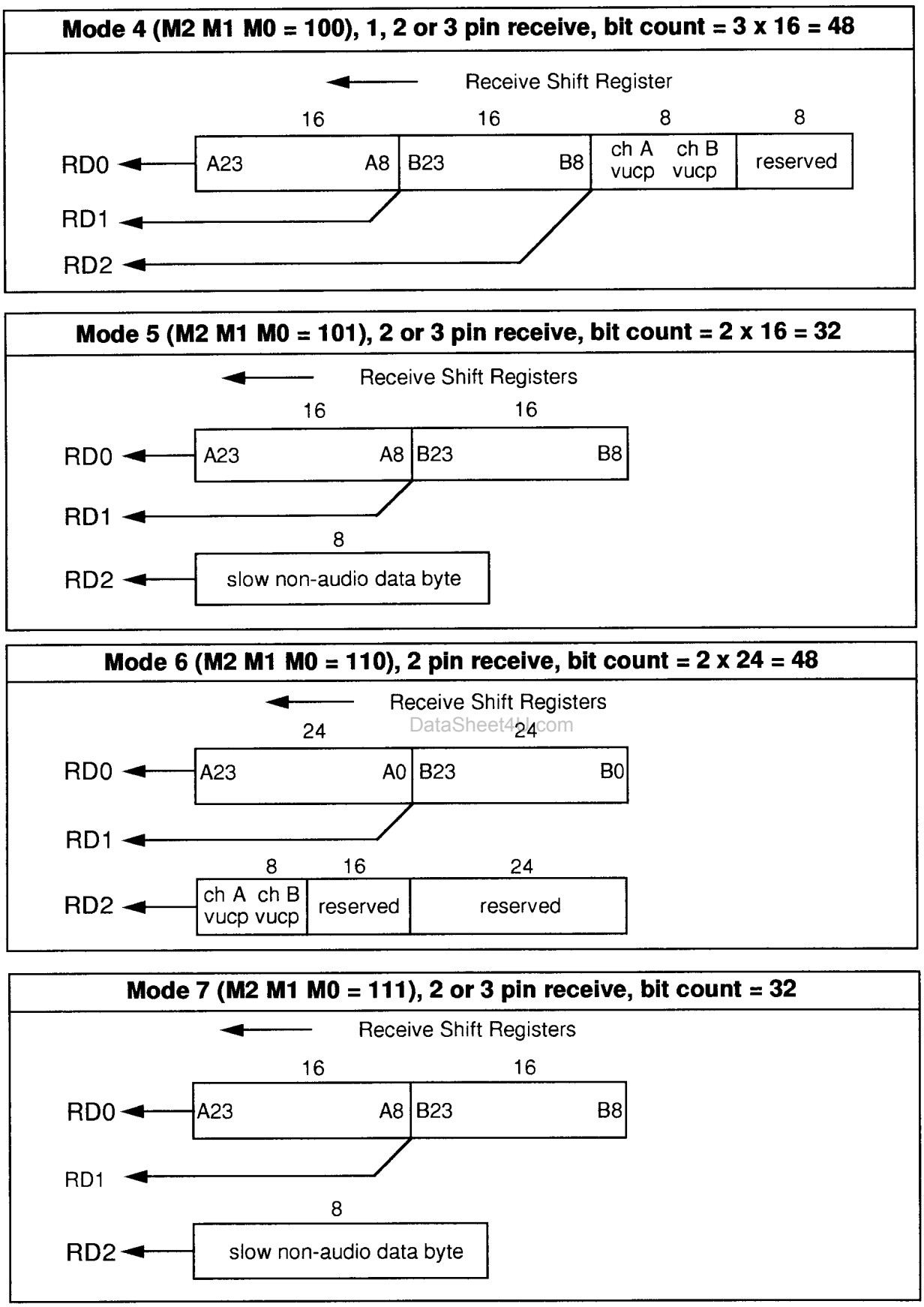


Figure 5-4 Receive Serial Modes (continued)

If the transmit CRC is enabled, the last 8 Ac bits in each block (frames 184-191) are ignored by the transmit modulator, which transmits a hardware-generated, channel A CRC byte in their place. If the transmit CRC is disabled, the last 8 Ac bits are transmitted in these positions. See Appendix B for more information on the CRC byte.

5.2.6 Channel B Channel Status (Bc) Bit

This bit is used to transmit the channel status bit for the channel B subframe. A block of 192 Bc bits forms the channel B channel status block defined by the digital audio transmission standard. Frame zero of the Bc bits must be synchronized with the transmit block sync (TBS) pin or by the transmit block reset command for proper alignment with the modulator preamble sync patterns.

If the transmit CRC is enabled, the last 8 Bc bits in each block (frames 184-191) are ignored by the transmit modulator, which transmits a hardware-generated, channel B CRC byte in their place. If the transmit CRC is disabled, the last 8 Bc bits are transmitted in these positions. See Appendix B for more information on the CRC byte.

5.2.7 Channel A Parity (Ap) and Channel B Parity (Bp) Bits

Since the transmit modulator provides hardware parity generation, the parity bit positions in the non-audio data are used to enter control information. Ap and Bp are encoded together as shown below. If the $\overline{\text{PRGE}}$ pin is deasserted high, Ap and Bp will not affect the program bits. If $\overline{\text{PRGE}}$ is asserted low, program bits (defined in Section 4.2) may be loaded at any time to select chip options. When Ap is set, Bp is shifted into a 24 bit program bit shift register. When Ap is cleared and the Ap of the two previous frames were set, the contents of the 24 bit temporary program word shift register are loaded into the 24 bit program word register to select chip options. Therefore, all 24 program bits should be loaded sequentially, P0 being the first bit and P23 being the last bit shifted in. If more than 24 program bits are loaded, only the last 24 bits are retained in the shift register. Ap and Bp may also be used to force a transmit block reset in which case the block start preamble will be transmitted in the frame following the frame in which the force transmit block reset command was received.

Ap	Bp	Parity Bit Meaning
0	0	No operation.
0	1	Force transmit modulator block reset.
1	0	Load program bit with Bp (zero).
1	1	Load program bit with Bp (one).

5.3 Receive Modes

The receive serial interface may be viewed as one, two or three shift registers clocked by RC (or RNS for the slow non-audio data modes), whose data is output through RD0, RD1 or RD2. In some modes, serial output pins may tap multiple points of the same shift register. This provides additional ways to use the receive serial interface. Figure 5-4 illustrates the pin usage, serial bit count, and bit ordering of each receive serial mode. Shift register fields shown as "reserved" read as zeroes.

5.4 Receive Non-Audio Data Format

Receive non-audio data consists of eight bits (one byte) per sample period (frame). Depending on the serial mode, the non-audio data may exit the DSP56401 on the same pin with audio sample data, or may exit through a separate pin. A "fast" non-audio mode (modes 0, 2, 4, 6) exists when the non-audio data is serially clocked by RC. A "slow" non-audio mode (modes 1, 3, 5, 7) exists when the non-audio data is serially clocked by RNS. Data clocked out of RD0 or RD1 is "fast" non-audio data and, except for serial mode 6, data clocked out of RD2 is "slow" non-audio data. Regardless of the serial rate or pin used, the non-audio data byte format is always the same.

Receive non-audio data is organized into blocks of 192 frames, numbered 0-191. The total non-audio information transferred each block is 192 bytes. The receive block sync (RBS) may be examined by the user to identify the first non-audio byte in a block. The meaning of each non-audio data byte in a block depends on its frame number relative to the

beginning of the block, as shown in Figure 5-5. Since Figure 5-5 represents physical shift registers which are shifted from right to left, the first bit exiting is on the left and the last bit exiting is on the right. In this section, the notation "Av" is used to indicate the "Channel A Validity" bit, and so on.

5.4.1 Channel A Validity (Av) Bit

This bit is cleared if the corresponding channel A audio sample is suitable for D/A conversion. Av is set if the corresponding channel A audio sample is unsuitable for D/A conversion. Av is typically used to mute the channel A audio.

5.4.2 Channel B Validity (Bv) Bit

This bit is cleared if the corresponding channel B audio sample is suitable for D/A conversion. Bv is set if the corresponding channel B audio sample is unsuitable for D/A conversion. Bv is typically used to mute the channel B audio.

5.4.3 Channel A User Data (Au) Bit

This bit is not defined by the AES, EBU or CP340 digital audio transmission standards and is available for user-specific features. Although block synchronization may be used, the Au bit has no restrictions on block size or serial protocol. The Au bit is defined in the Compact Disc format and is also used in AES18-1992 (ANSI S4.52-1992) "AES Recommended Practice for Digital Audio Engineering — Format for the User Data Channel of the AES Digital Audio Interface", Au should be set to zero.

5.4.4 Channel B User Data (Bu) Bit

This bit is not defined by the AES, EBU or CP340 digital audio transmission standards and is available for user-specific features. Although block synchronization may be used, the Bu bit has no restrictions on block size or serial protocol. The Bu bit is defined in the Compact Disc format and is also used in AES18-1992 (ANSI S4.52-1992) "AES Recommended Practice for Digital Audio Engineering — Format for the User Data Channel of the AES Digital Audio Interface", Bu should be set to zero.

5.4.5 Channel A Channel Status (Ac) Bit

This bit is used to receive the channel status bit for the channel A subframe. A block of 192 Ac bits forms the channel A channel status block defined by the digital audio transmission standard. Frame 191 of the Ac bits is synchronized with the receive block sync (RBS) pin.

The last 8 Ac bits in each block (frames 184-191) are not output by the receive serial interface. The receive demodulator always interprets these bits as the channel A CRC byte, which is checked for errors by the receive hardware. The channel A CRC error is indicated by status bit S14. Frames 184-191 are used to output 8 status bits (S0, S2, S4, S6, S8, S10, S12 and S14) instead of the 8 Ac or CRC bits. S0 is the first bit and S14 is the last bit shifted out. The timing is detailed in Figure 5-5 and Figure 6-10.

5.4.6 Channel B Channel Status (Bc) Bit

This bit is used to receive the channel status bit for the channel B subframe. A block of 192 Bc bits forms the channel B channel status block defined by the digital audio transmission standard. Frame 191 of the Bc bits is synchronized with the receive block sync (RBS) pin.

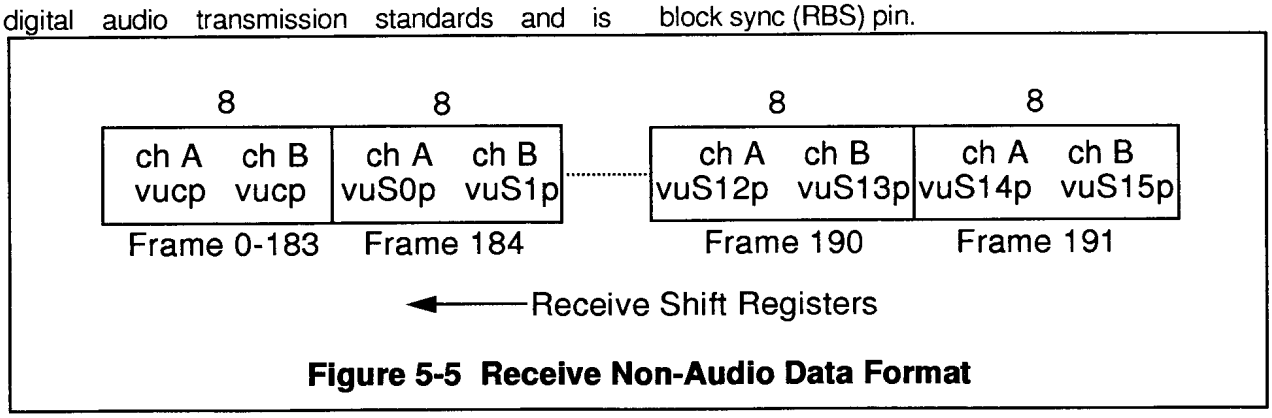


Figure 5-5 Receive Non-Audio Data Format

The last 8 Bc bits in each block (frames 184-191) are not output by the receive serial interface. The receive demodulator always interprets these bits as the channel B CRC byte, which is checked for errors by the receive hardware. A channel B CRC error is indicated by status bit S15. Frames 184-191 are used to output 8 status bits (S1, S3, S5, S7, S9, S11, S13 and S15) instead of the 8 Bc or CRC bits. S1 is the first bit and S15 is the last bit shifted out. The timing is detailed in Figure 5-5 and Figure 6-10.

5.4.7 Channel A Parity (Ap) Bit

This bit indicates a hardware-detected parity error in the corresponding channel A subframe. If Ap is cleared, the channel A subframe had no parity error. If Ap is set, a parity error was detected in the channel A subframe.

5.4.8 Channel B Parity (Bp) Bit

This bit indicates a hardware-detected parity error in the corresponding channel B subframe. If Bp is cleared, the channel B subframe had no parity error. If Bp is set, a parity error was detected in the channel B subframe.

5.4.9 Status (S0-S15) Bits

These bits monitor chip operation and communicate error conditions. S0-S15 are defined in Section 4.3.

Electrical Timing

This section describes the DSP56401 electrical timing parameters. All input pin timing is specified to TTL levels (V_{ih} and V_{il}) unless otherwise noted. All output pin timing is specified to CMOS levels (V_{ohc} and V_{olc}) unless otherwise noted. $V_{ohc} = V_{cc}$-0.1 V, V_{olc} = 0.1 V.

6.1 Maximum Ratings (V_{ss} = 0 V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{cc}	-0.3 to +7.0	V
Pin Voltage	V_{in} or V_{out}	-0.5 to V_{cc}+0.5	V
Operating Temperature	T_a	0 to +70	°C
Storage Temperature	T_{stg}	-50 to +150	°C
Lead Temperature (10 sec. soldering)	T_l	300	°C

This device contains circuitry to protect the pins from high static voltages and electric fields. However, for proper operation and long term reliability it is recommended that all pin voltages be constrained to the range $V_{ss} < (V_{in}$ or $V_{out}) < V_{cc}$. Unused inputs must be tied to either V_{ss} or V_{cc}.

6.2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance - Plastic PLCC	θ_{ja}	51	°C/W

6.3 DC Electrical Characteristics

(V_{ss} = 0 V, V_{cc} = 5.0 V+10%, T_a = 0 to +70 C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage (except OSCIN0-3)	V_{ih}	2.0	-	V_{cc}	V
Input Low Voltage (except OSCIN0-3)	V_{il}	0.0	-	0.8	V
Input High Voltage (OSCIN0-3)	V_{ihc}	3.85	-	V_{cc}	V
Input Low Voltage (OSCIN0-3)	V_{ilc}	0.0	-	1.35	V
Input Leakage Current	I_{in}	-10	-	10	µA
Three-State (Off) Output Current	I_{tsi}	-10	-	10	µA
Open Drain Output Leakage Current	I_{odi}	-10	-	10	µA
Output High Current (Voh = 3.7 V)	I_{ol}	-4.0	-	-	mA
Output Sink Current (Vol = 0.4 V)	I_{oh}	4.0	-	-	mA
Power Dissipation (see Note 1)	P_d	-	150	-	mW
Power Dissipation (see Note 2)	P_s	-	1	-	mW
Input Capacitance (see Note 3)	C_{in}	-	10	-	pF
Output Capacitance (see Note 3)	C_{out}	-	12.5	-	pF
I/O Capacitance (see Note 3)	C_{io}	-	15	-	pF

6.4 AC Electrical Characteristics - Clock Timing (C_L=50 pF)

Num.	Characteristic	Min	Max	Unit
1	OSCIN0-3 Cycle Period	20	-	ns
1a	OSCIN0-3 Frequency	-	50	MHz
1b	OSCIN0-3 Duty Cycle (see Note 4)	45	55	%
2	OSCIN0-3 High	10	-	ns
3	OSCIN0-3 Low	10	-	ns
4	PTC, PRC Cycle Period	40	-	ns
4a	PTC, PRC Frequency	-	25	MHz
5	PTC, PRC High	10	-	ns
6	PTC, PRC Low	20	-	ns
7	PTC, PRC Delay From OSCIN0-3, TC	20	100	ns

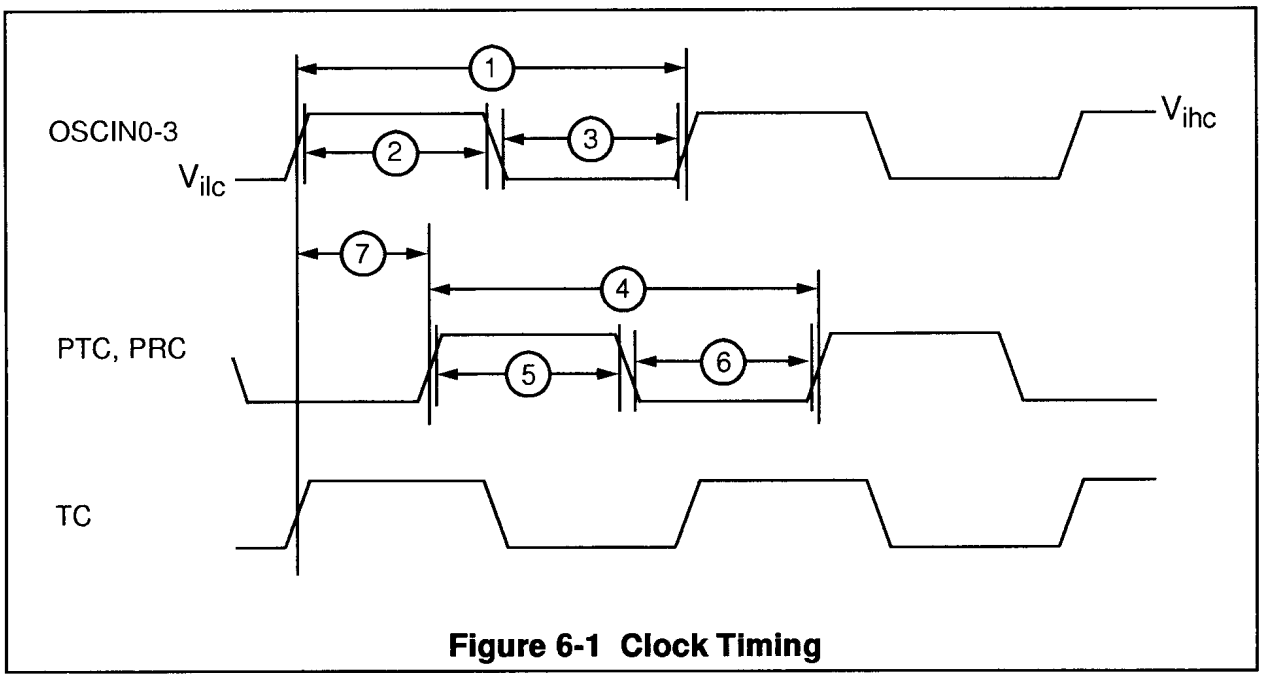


Figure 6-1 Clock Timing

6.5 AC Electrical Characteristics - Transmit Serial Interface Timing

(CL = 50 pF)

Num.	Characteristic	Min	Max	Unit
10	TC Cycle Time (see Note 5)	80	-	ns
10a	TC Frequency	-	12.5	MHz
10b	TC Duty Cycle (see Note 6)	45	55	%
11	TC High	35	-	ns
12	TC Low	35	-	ns
13	TSI Setup Time To TC	5	-	ns
14	TSI Hold Time From TC	10	-	ns
15	$\overline{\text{TWI}}$ Setup Time To TC	5	-	ns
16	$\overline{\text{TWI}}$ Hold Time From TC	10	-	ns
17	TD0-1 Setup Time To TC	5	-	ns
18	TD0-1 Hold Time From TC	10	-	ns
19	TSO Assertion From TC	-	35	ns
20	TSO Negation From TC	-	35	ns
21a	TSO Assertion To TFS Assertion (see Note 9)	6TC	-	cyc
21b	TSO Assertion to TFS Assertion (see Note 10)	0TC	-	cyc
21c	TSO Assertion to TFS Assertion (see Note 11)	0TC	-	cyc
22	TBS Assertion or Negation From TC	-	35	ns
23	TFS Assertion From TC	-	35	ns
24	TFS Negation From TC	-	35	ns
25	TNS Enable From TC	-	35	ns
26	TNS Disable From TC	-	35	ns
27	TNS Low From TC	-	35	ns
28	TNS High From TC	-	35	ns

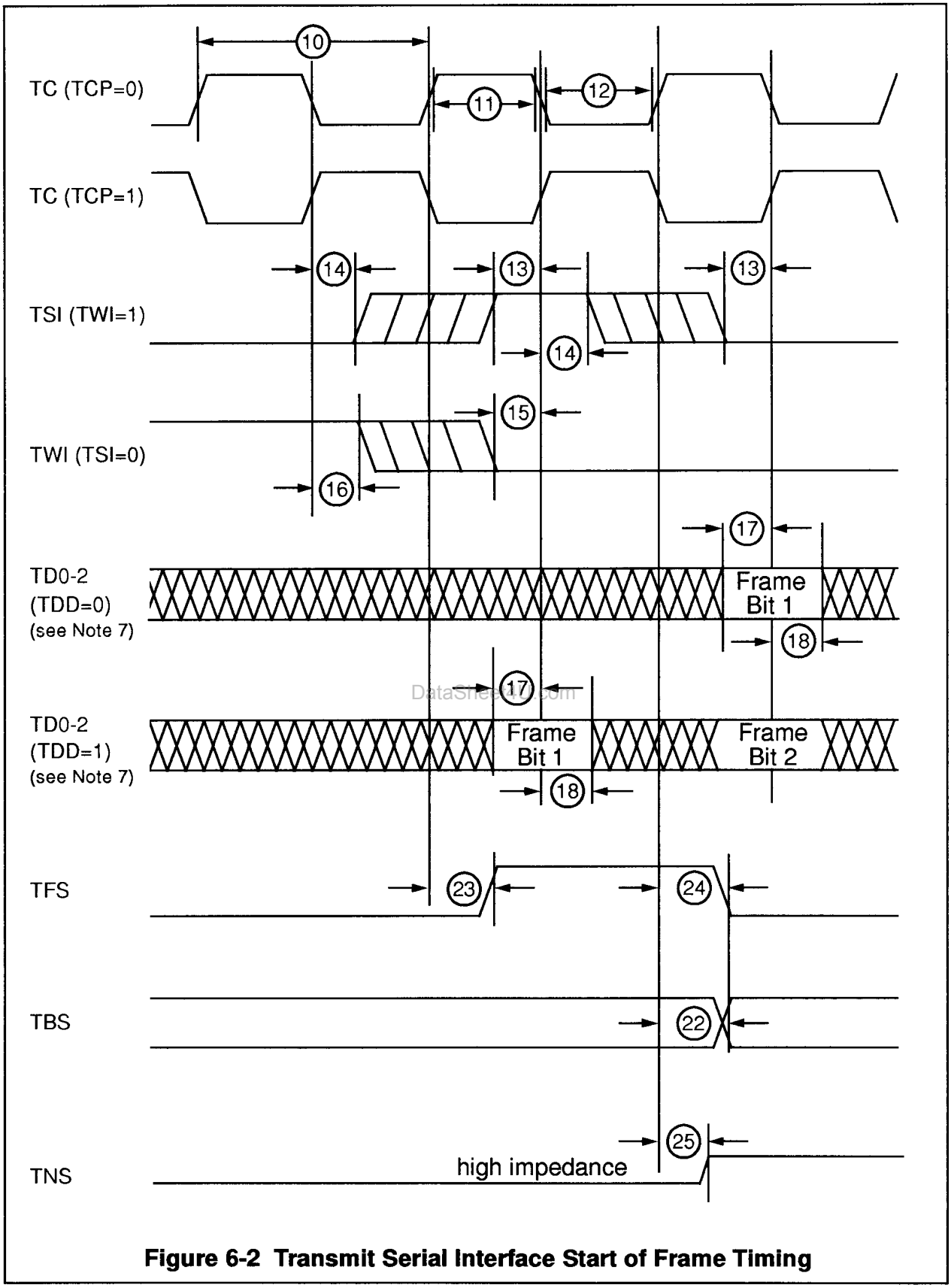


Figure 6-2 Transmit Serial Interface Start of Frame Timing

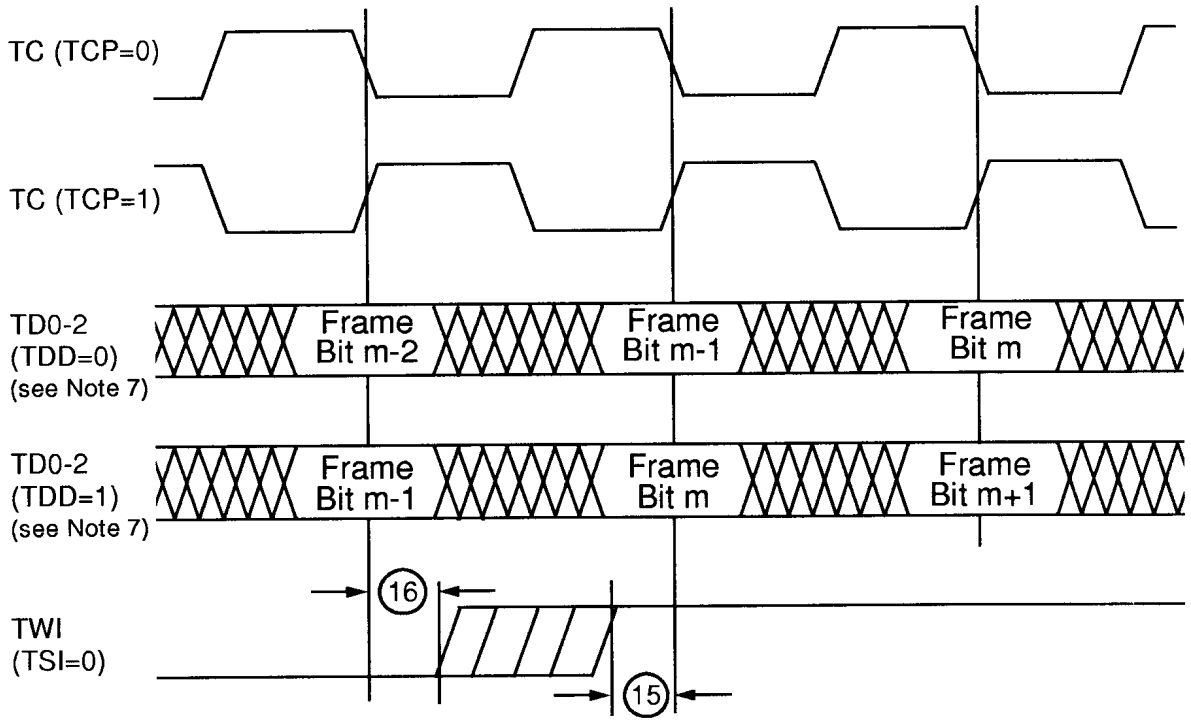


Figure 6-3 Transmit Serial Interface Middle of Frame Timing (Contiguous Data)

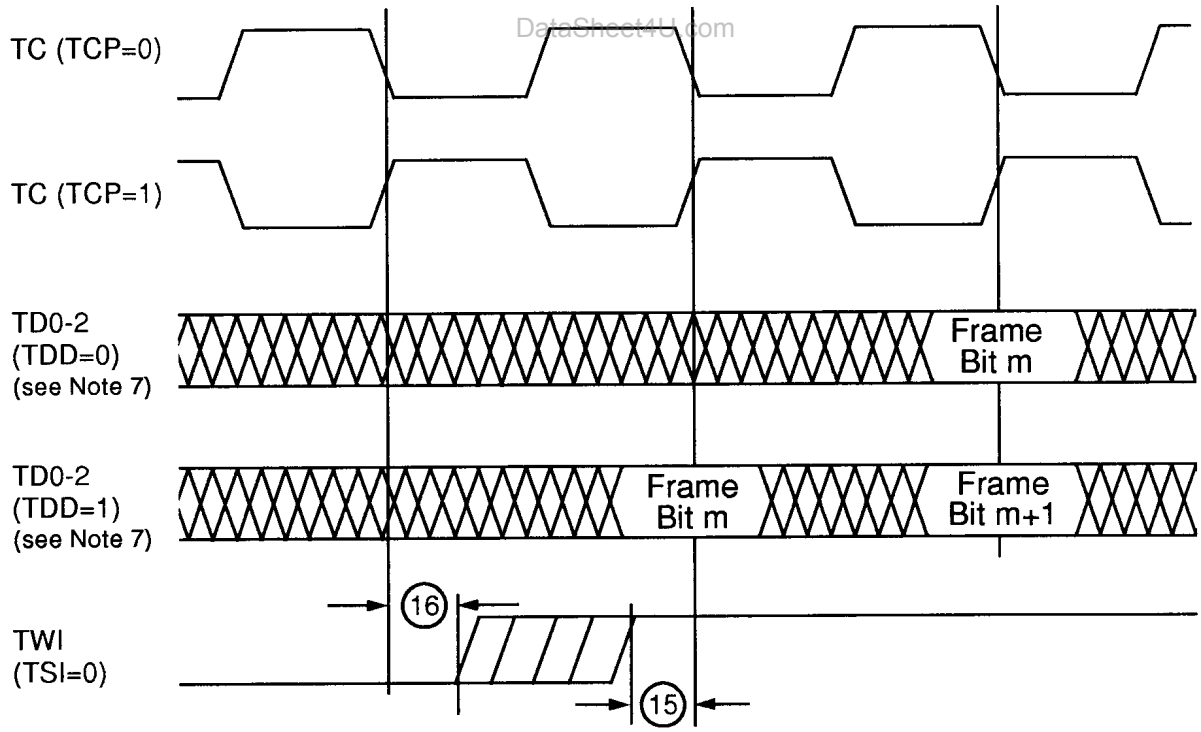


Figure 6-4 Transmit Serial Interface Middle of Frame Timing (Noncontiguous Data)

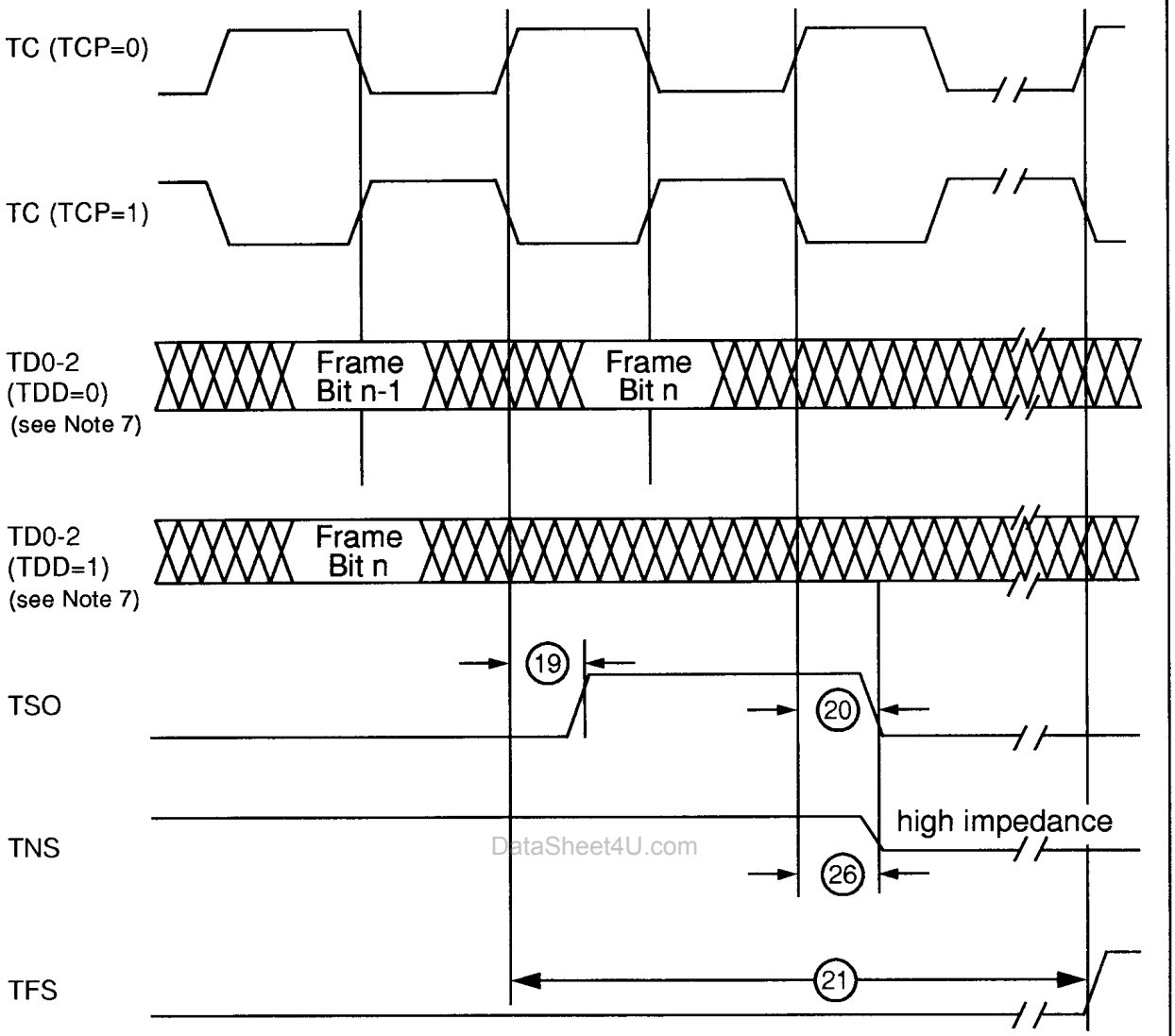


Figure 6-5 Transmit Serial Interface End of Frame Timing

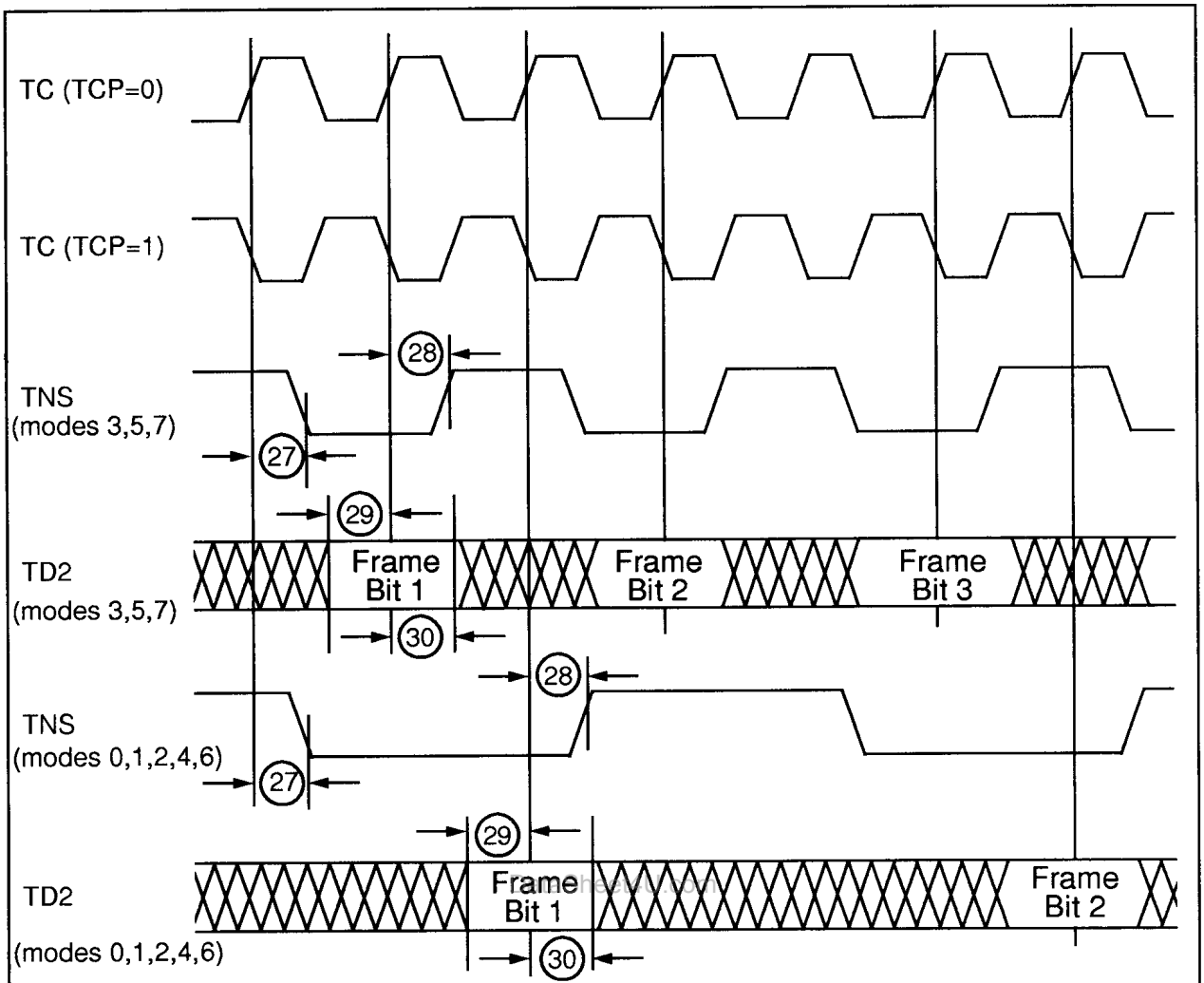


Figure 6-6 Transmit Serial Interface Non-Audio Data Timing

6.6 AC Electrical Characteristics - Receive Serial interface Timing (C_L=50pF)

Num.	Characteristic	Min	Max	Unit
40	RC Cycle Period (see Note 12)	80	-	ns
40a	RC Frequency	-	12.5	MHz
41	RC High	35	-	ns
42	RC Low	35	-	ns
43	RSI Setup Time To RC	5	-	ns
44	RSI Hold Time From RC	10	-	ns
45	RD0-2 Enable From RC	-	35	ns
46	RD0-2 Disable From RC	-	35	ns
47	RD0-2 Valid From RC	-	35	ns
48	RSO Assertion From RC	-	35	ns
49	RSO Negation From RC	-	35	ns
50	RSO Assertion To RFS Assertion	0RC	-	cyc
51	RBS Assertion or Negation From RC	-	35	ns
52	RFS Assertion From RC	-	35	ns
53	RFS Negation From RC	-	35	ns
54	RWS0-1 Low From RC	-	35	ns
55	RWS0-1 High From RC	-	35	ns
56	RNS Enable From RC	-	35	ns
57	RNS Disable From RC	-	35	ns
58	RNS Low From RC	-	35	ns
59	RNS High From RC	-	35	ns

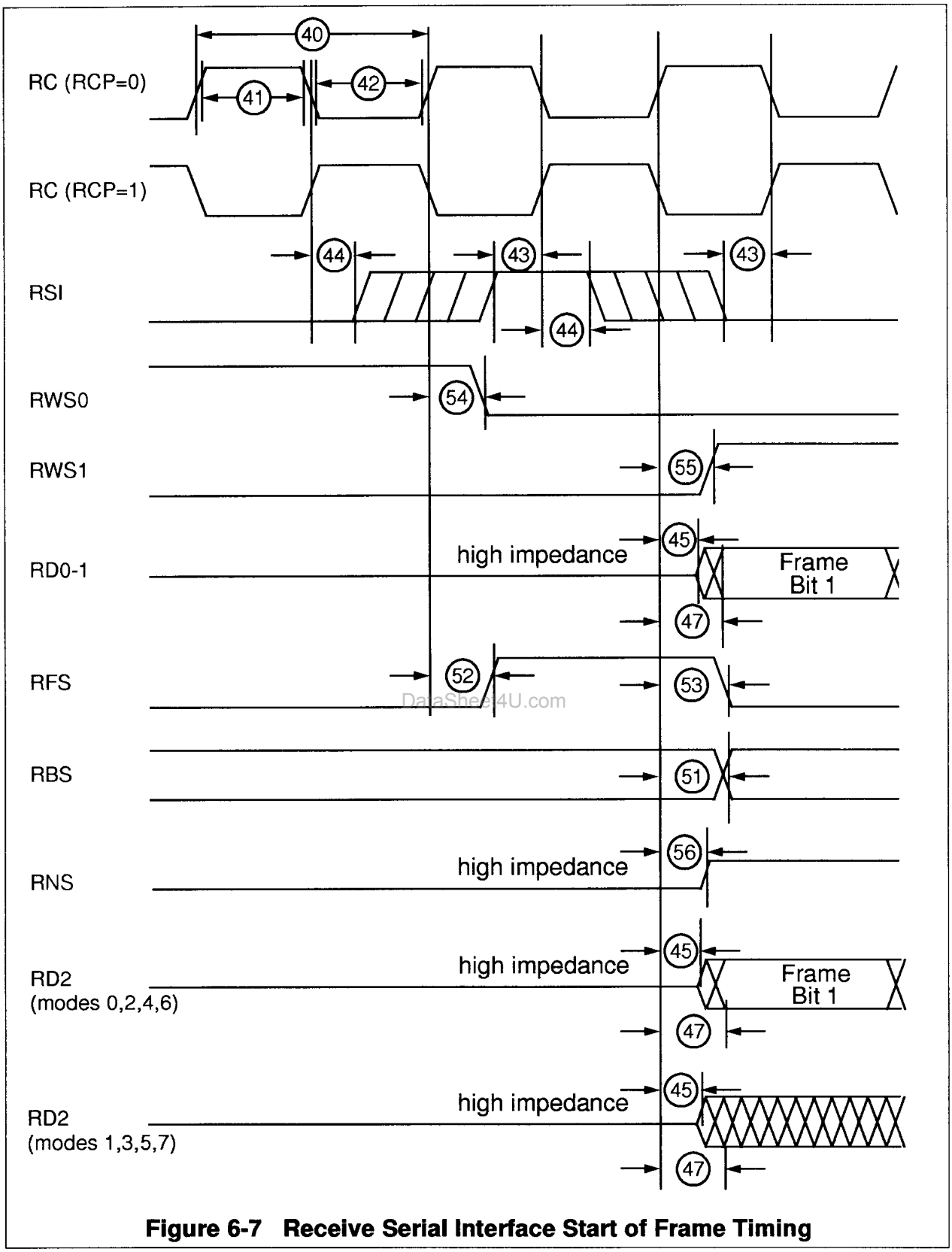


Figure 6-7 Receive Serial Interface Start of Frame Timing

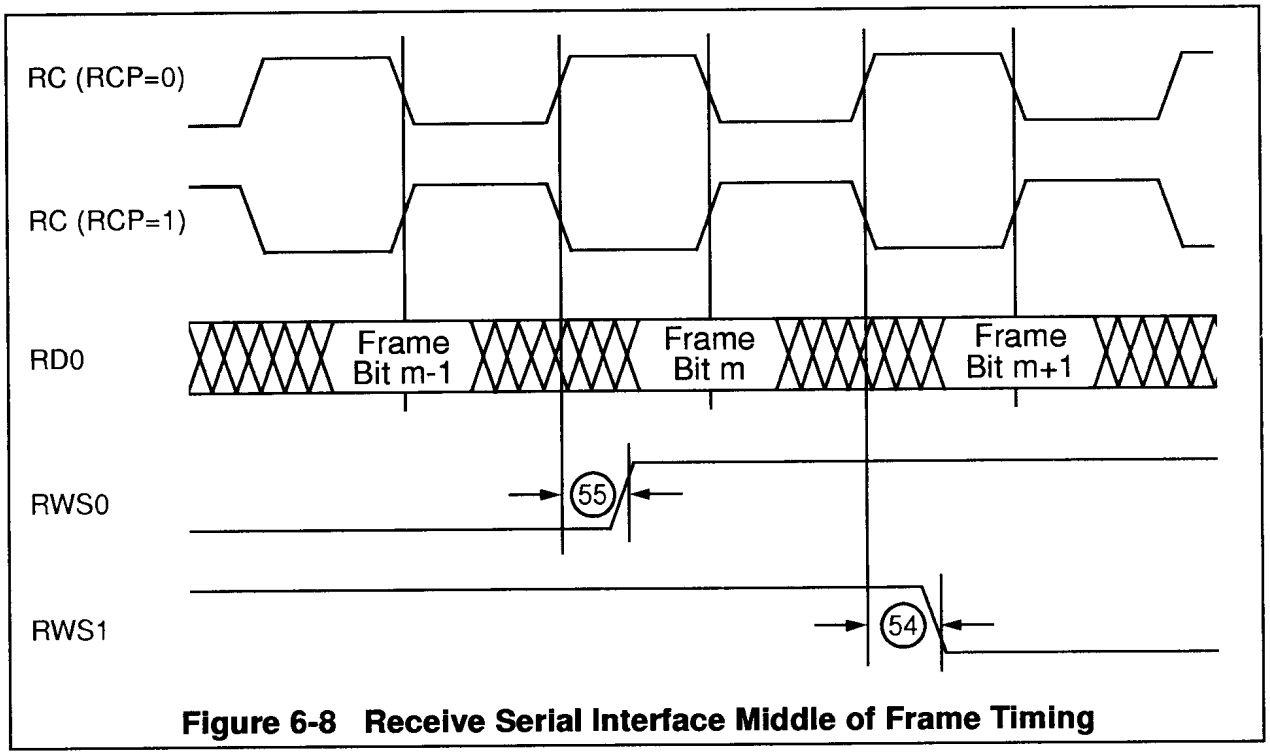


Figure 6-8 Receive Serial Interface Middle of Frame Timing

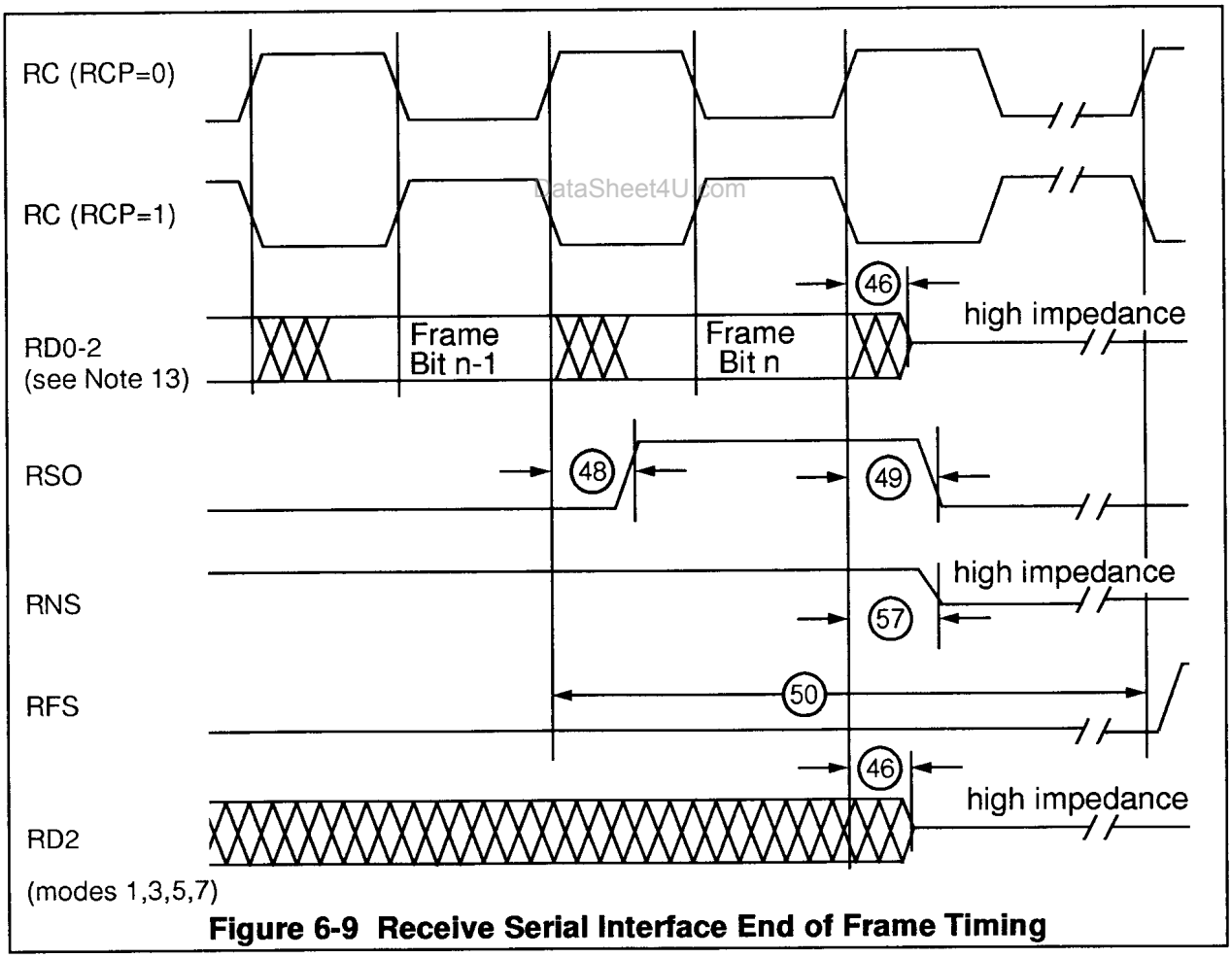


Figure 6-9 Receive Serial Interface End of Frame Timing

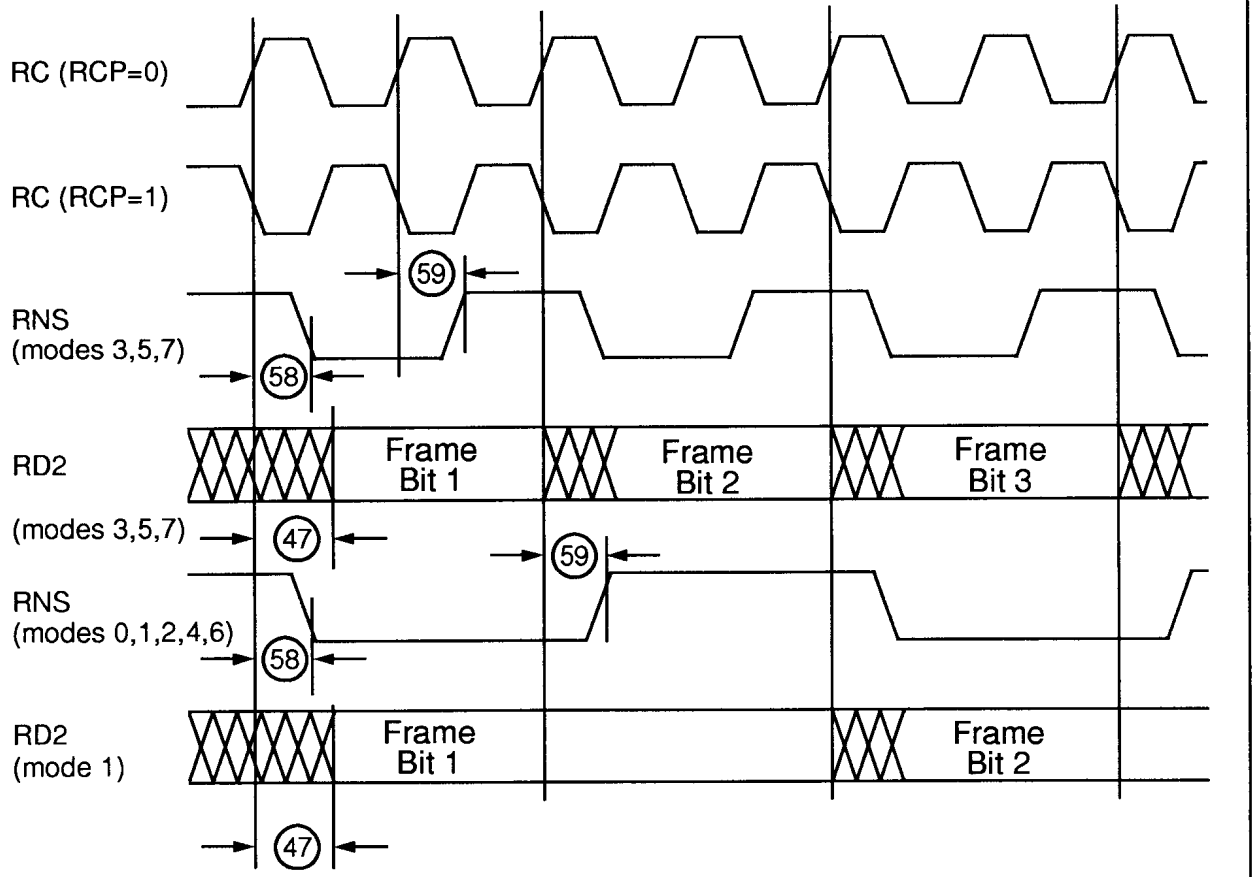


Figure 6-10 Receive Serial Interface Non-Audio Data Timing

6.7 AC Electrical Characteristics - $\overline{TOE}$, $\overline{ROE}$ Timing

(C_L=50 pF)

Num.	Characteristic	Min	Max	Unit
70	TFS,TBS,MSO,PTC Enable From $\overline{TOE}$	-	35	ns
71	TFS,TBS,MSO,PTC Disable From $\overline{TOE}$	-	35	ns
72	RFS,RWS0-1,RBS,LOCK,PRC Enable From $\overline{ROE}$	-	35	ns
73	RFS,RWS0-1,RBS,LOCK,PRC Disable From $\overline{ROE}$	-	35	ns

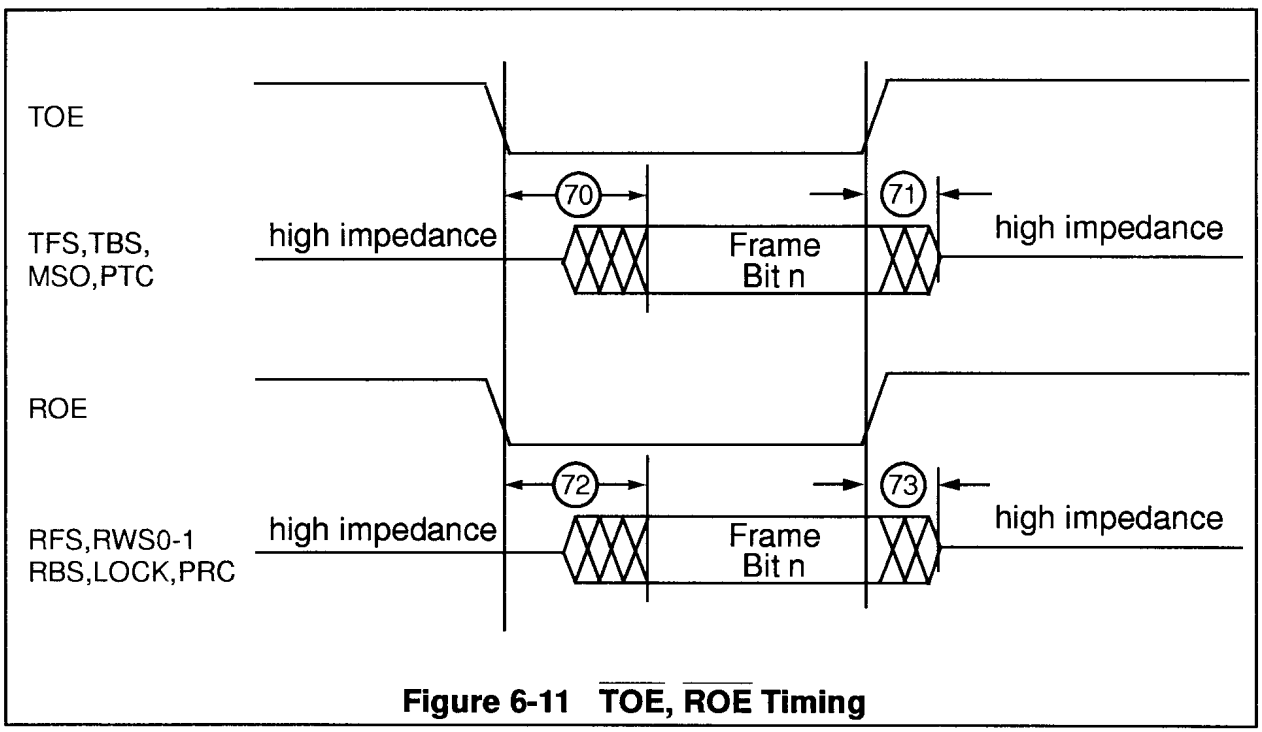


Figure 6-11 $\overline{TOE}$, $\overline{ROE}$ Timing

6.8 AC Electrical Characteristics - Modulator Timing

(C_L=50 pF)

Num.	Characteristic	Min	Max	Unit
80	MSI Setup Time To Clock	0	-	ns
81	MSI Hold Time From Clock	15	-	ns
82	$\overline{\text{MWI}}$ Setup Time To Clock	0	-	ns
83	$\overline{\text{MWI}}$ Hold Time From Clock	15	-	ns
84	MSO Assertion From Clock	-	40	ns
85	MSO Negation From Clock	-	40	ns

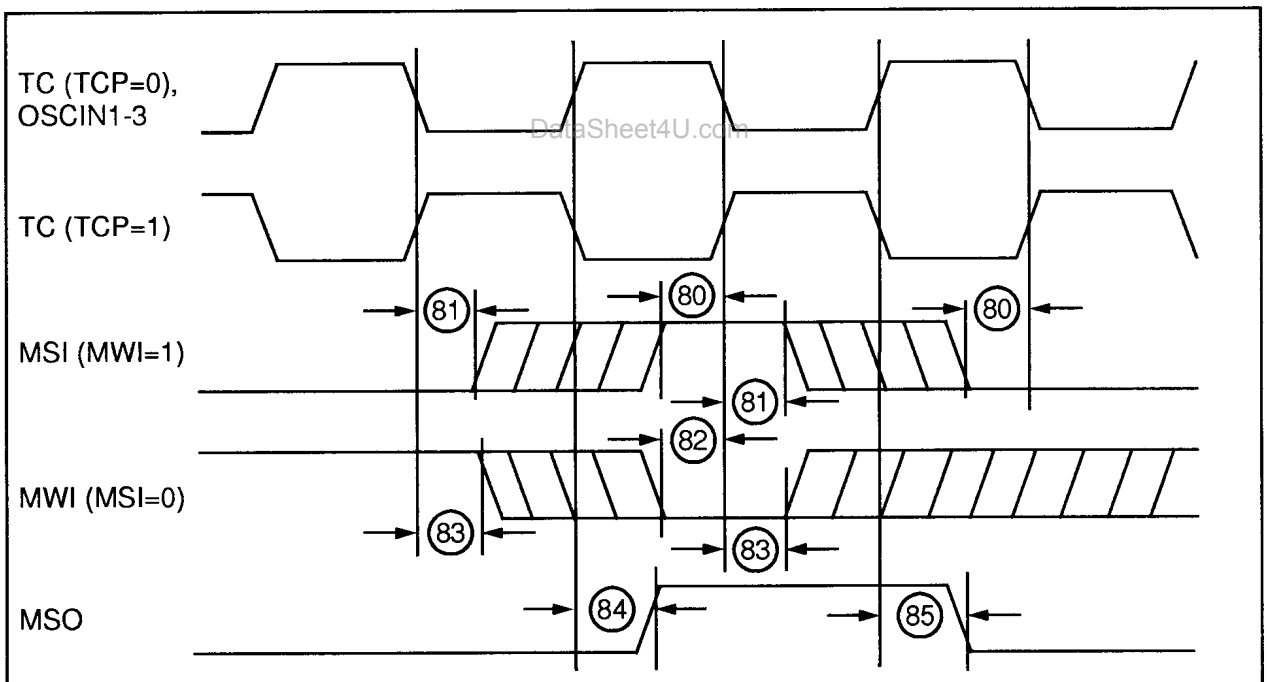


Figure 6-12 Modulator Timing (see Note 14)

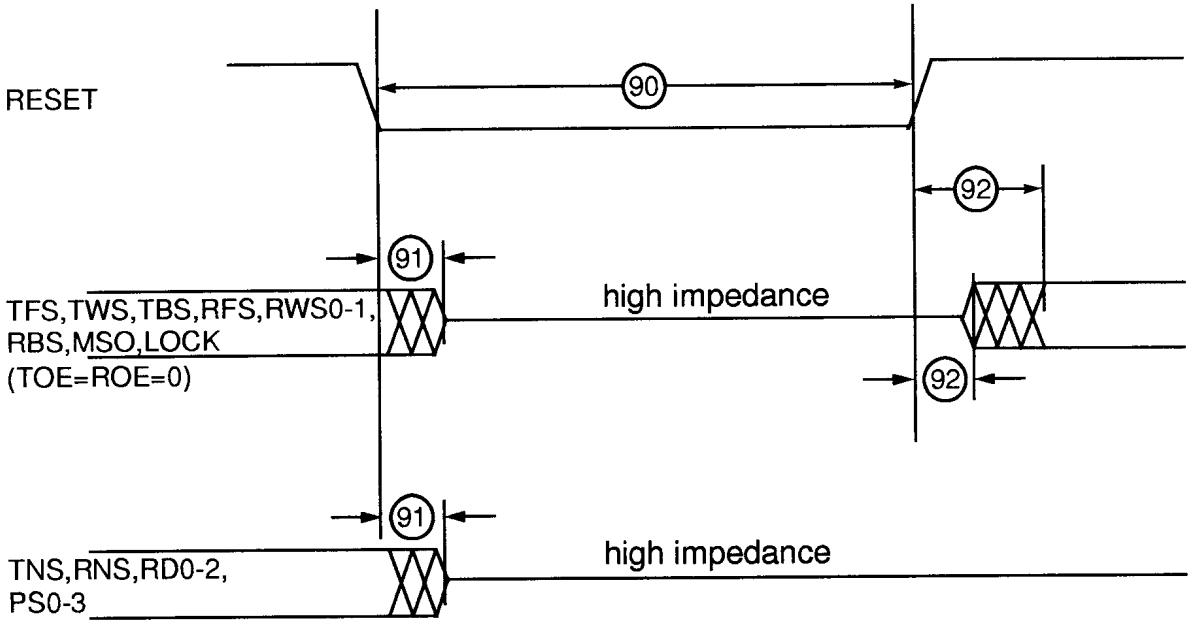


Figure 6-13 $\overline{\text{RESET}}$ Timing

6.9 AC Electrical Characteristics - $\overline{\text{RESET}}$ Timing

(C_L=50 pF)

Num.	Characteristic	Min	Max	Unit
90	$\overline{\text{RESET}}$ Assertion	15	-	ns
91	Output Disable From $\overline{\text{RESET}}$	-	35	ns
92	Output Enable From $\overline{\text{RESET}}$	-	35	ns

Note 1 – OSCIN0 frequency is 12.288 MHz, TC and RC frequency is 6.144 MHz, modulator locked to demodulator, $V_{ih} > V_{cc}$ - 0.2 V, $V_{il} < 0.2$ V, 50 pF loads, no DC loads. Other oscillators are off.

Note 2 – All oscillators off, TC and RC off, $V_{ih} > V_{cc}$ - 0.2 V, $V_{il} < 0.2$ V, $V_{ihc} > V_{cc}$ - 0.2 V, $V_{ilc} < 0.2$ V, no DC loads.

Note 3 – Not tested in production.

Note 4 – The OSCIN0-3 duty cycle is important only if OSCIN0-3 directly drives the transmit modulator clock (TMCLK), or drives the receive demodulator clock (RDCLK) through the 2X frequency doubler or the divide by 1.5 circuits. See Section 4.2 for more details.

Note 5 – Many applications use PTC (or PRC) to clock TC, either directly or through external dividers or sigma delta data converters. For jitter-free TFS operation, there is a maximum external delay in the PTC (or PRC) to TC path. If TC has less than 64 clock periods per frame sync, the maximum external delay is 1/TMCLK - 50 ns. If TC has more than 64 clock periods per frame sync, the maximum external delay is 1/TC - 50 ns.

Note 6 – The TC duty cycle is important only if TC directly drives the transmit modulator clock (TMCLK). The TMCLK duty cycle should be nominally 50 percent. See Sections 2.5 and 4.2 for more details.

Note 7 – Applies to TD2 only in serial mode 6.

Note 8 – Applies to TD2 in serial modes other than mode 6.

Note 9 – Applies in serial modes 1, 5, and 6 when the transmit modulator is a free running master operating asynchronous to the transmit serial interface.

Note 10 – Applies in serial modes 0, 2, 3, 4 and 7 when the transmit modulator is a free running master operating asynchronous to the transmit serial interface.

Note 11 – Applies in all serial modes when transmit modulator is a slave locked synchronously to the transmit serial interface. Synchronous operation occurs when TC and TMCLK are derived from the same clock source, and TSI and MSI are connected together ($\overline{TWI}$ = $\overline{MWI}$ = 1) or $\overline{TWI}$ and $\overline{MWI}$ are connected together (TSI=MSI=0).

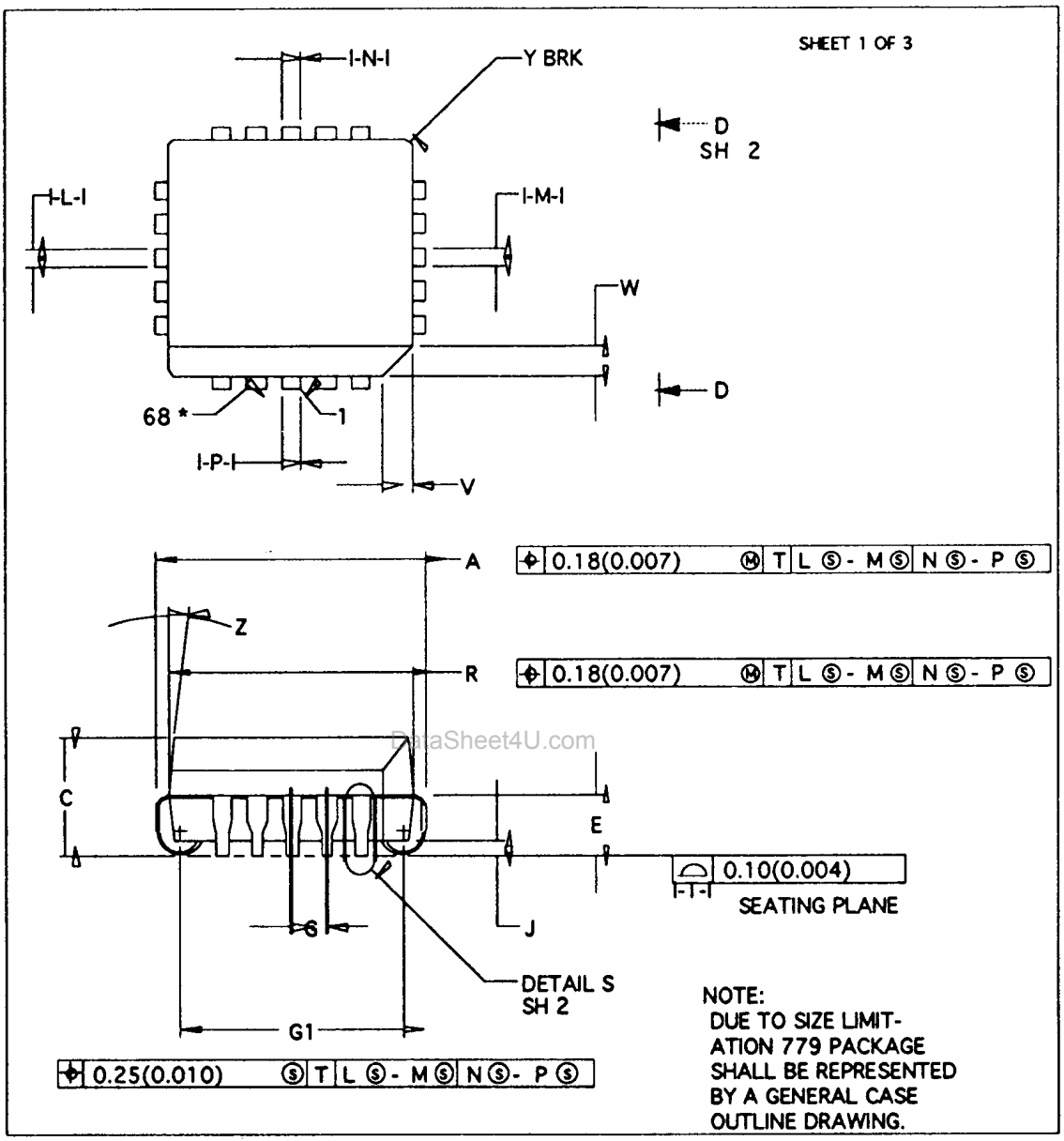
Note 12 – Many applications use PRC (or PTC) to clock RC, either directly or through external dividers or sigma delta converters. For jitter-free RFS operation, there is a maximum external delay in the PRC (or PTC) to RC path. If RC has less than 64 clock periods per frame sync, the maximum external delay is 8/RDCLK - 50 ns. If RC has more than 64 clock periods per frame sync, the maximum external delay is 1/RC - 50 ns

Note 13 – Applies to RD2 only in serial modes 0, 2, 4 and 6.

Note 14 – When program bits P12-P10 = 000, MSO changes synchronous to the rising edges of the internal "RDCLK ÷ 8" clock (refer to Figure 2-6); this "RDCLK ÷ 8" clock may be chosen as the output of the PRC and PTC pins. MSI is ignored when P12-P10 = 000.

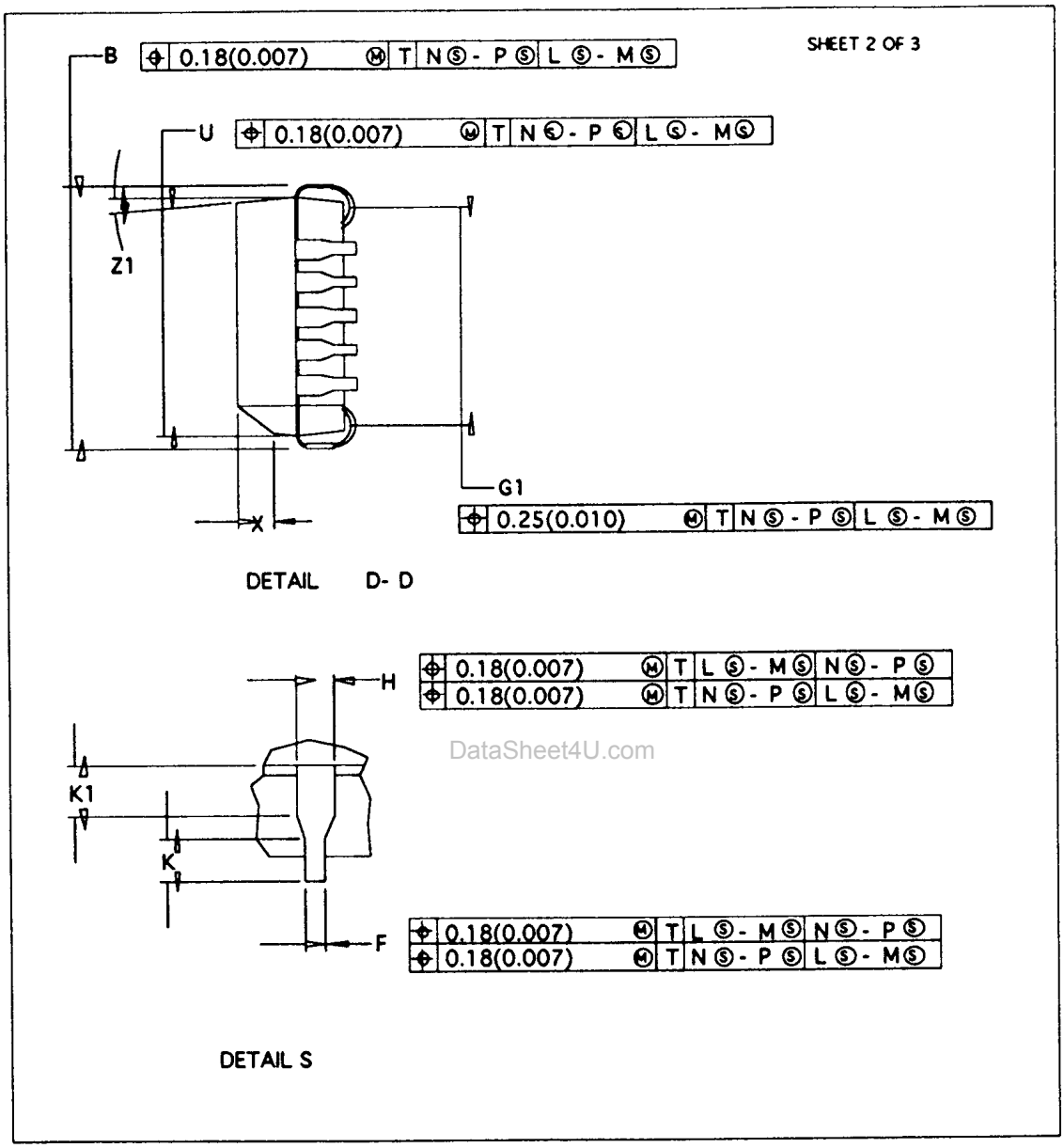
Table 1: DSP56401 Pinout (80 Pin QFP)

PIN #	DESCRIPTION	PIN #	DESCRIPTION	PIN #	DESCRIPTION	PIN #	DESCRIPTION
1	RWS0	21	D2	41	$\overline{PS}$	61	H5
2	RBS	22	D1	42	$\overline{DS}$	62	H6
3	TNS	23	D0	43	X/$\overline{Y}$	63	INTERNAL LOGIC VCC
4	$\overline{RESET}$	24	A14	44	$\overline{RD}$	64	H7
5	PTC	25	A13	45	$\overline{WR}$	65	$\overline{HREQ}$
6	TC	26	A12	46	$\overline{BR}$	66	HR/$\overline{W}$
7	TCP	27	A11	47	SRD	67	$\overline{HEN}$
8	VSSB	28	ADDRESS BUS GND	48	SC1	68	$\overline{HACK}$
9	VDDB	29	A10	49	STD	69	HA0
10	DATA BUS VCC	30	A9	50	SC2	70	HA1
11	D11	31	A8	51	INTERNAL LOGIC VCC	71	HA2
12	D10	32	A7	52	INTERNAL LOGIC GND	72	INTERNAL LOGIC GND
13	D9	33	A6	53	SCK	73	INTERNAL LOGIC VCC
14	D8	34	ADDRESS BUS VCC	54	SC0	74	EXTAL
15	D7	35	A5	55	H0	75	$\overline{RESET}$
16	D6	36	A4	56	INTERNAL LOGIC GND	76	$\overline{IRQA}$/MODA
17	DATA BUS GND	37	A3	57	H1	77	D23
18	D5	38	A2	58	H2	78	D22
19	D4	39	A1	59	H3	79	D21
20	D3	40	A0	60	H4	80	D20



CASE NO.	779-02
STATUS	MOTOROLA STANDARD
NEW STD	
USED ON	MOS/BI POLAR (68 LEAD) PLASTIC LEADED CHIP CARRIER W/O PEDESTAL

Mechanical Specification Figure 1. Quad Flat Pack



CASE NO.	779-02
STATUS	MOTOROLA STANDARD
NEW STD	
USED ON	MOS/BI POLAR (68 LEAD) PLASTIC LEADED CHIP CARRIER W/O PEDESTAL

Mechanical Specification Figure 1. Quad Flat Pack (Continued)

NOTES

1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25(0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. 779-01 OBSOLETE, NEW STANDARD 779-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.02	25.27	0.985	0.995
B	25.02	25.27	0.985	0.995
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	---	0.020	---
K	0.64	---	0.025	---
R	24.13	24.28	0.950	0.956
U	24.13	24.28	0.950	0.956
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	---	0.50	---	0.020
Z	2°x127	10°x127	2°x127	10°x127
G1	23.12	23.62	0.910	0.930
K1	1.02	---	0.040	---
Z1	2°x127	10°x127	2°x127	10°x127

CASE NO.	779-02
STATUS	MOTOROLA STANDARD
NEW STD	
USED ON	MOS/BI POLAR (68 LEAD) PLASTIC LEADED CHIP CARRIER W/O PEDESTAL

Mechanical Specification Figure 1. Quad Flat Pack (Continued)

Digital Applications Hardware

This section presents applications diagrams and timing for several example systems. There are many hardware variations which will work and not all are shown here. It is also possible to mix ideas from several examples.

The wiring diagrams do not include every DSP56401 pin. They do include every transmit serial interface and receive serial interface pin as well as selected pins from the transmit modulator, receive demodulator and clock generation and control sections. The digital audio interfaces and analog/PLL circuits are covered in more detail in Section 8.

7.1 DSP56401 Initialization

The DSP56401 requires a hardware reset to clear the program word to its reset state. If PTC or PRC is needed by other devices during reset, $\overline{TOE}$ or $\overline{ROE}$ should be asserted during $\overline{RESET}$ assertion to enable the PTC or PRC output. In a multiple DSP56401 system, only one $\overline{TOE}$ and $\overline{ROE}$ should be asserted at a time. The DSP56401 reset state is an initial hardware configuration which allows most applications to start without difficulty. Upon $\overline{RESET}$, the DSP56401 program word is cleared to all zeroes. This yields a clock generation and control reset state which exists until the application can load the desired program word. The reset state is listed in Figure 7-1.

An application's ability to load an initial program word depends on its hardware schematic. Difficulties loading the program word after $\overline{RESET}$ fall into several categories.

1. The DSP56001 and DSP56156 SSI bit clock rate cannot exceed one-fourth the DSP56001/DSP56002/DSP56156 clock frequency. If PTC is directly connected to the SSI clock, the reset state permits the maximum OSCIN0 frequency to be eight times the maximum SSI clock frequency, or twice the DSP clock frequency. If PRC is directly connected to the SSI clock, the reset state permits the maximum OSCIN0 frequency to be four times the maximum SSI clock frequency, or equal to the DSP clock frequency.

2. The minimum number of TC clocks per transmit modulator frame sync (TFS) cannot be less than the serial mode bit count. Too few TC clocks may cause DSP56401 to be unable to load the program bits or may cause the SSI to miss frame syncs and boundaries. The designer should be careful not to violate this requirement when a Sigma-Delta data converter divides down PTC or PRC to generate the SSI clock.

3. If PTC or PRC directly drives an input clock of a Sigma-Delta data converter, the number of PTC or PRC clocks per frame sync should be appropriate for that converter's internal state machine.

4. The device that programs the DSP56401 must ensure that it provides 24 contiguous frames with

- Transmit modulator sample rate - OSCIN0 divided by 1024.
- Programmable transmit clock (PTC) rate - OSCIN0 divided by 8. Relative to the transmit modulator sample rate, this is a 128X clock.
- Transmit serial interface bit rate - TC input rate. The serial mode bit count is the minimum number of TC clocks per transmit frame sync (TFS).
- Receive demodulator sample rate - OSCIN0 divided by 1024.
- Programmable receive clock (PRC) rate - OSCIN0 divided by 4. Relative to the receive demodulator sample rate, this is a 256X clock.
- Receive serial interface bit rate - RC input rate. The serial mode bit count is the minimum number of RC clocks per receive frame sync (RFS).

Figure 7-1 Reset State

Ap set followed by at least one frame with Ap cleared in order to load a new program word. The $\overline{PRGE}$ pin, when high, prevents the loading of program bits, may be held high until it is time to program the DSP56401 to provide an extra measure of security, must be pulled low to load program bits. After the second frame with Ap cleared, $\overline{PRGE}$ may be returned high.

5. When a new program word is loaded, PTC and PRC may exhibit glitches if their clock sources are switched and an extra or narrow clock pulse may occur. When PTC or PRC feed TC or RC, the DSP56401 will recover from any clock glitches by the next frame sync. If a device connected to the DSP56401 cannot recover from a clock glitch, it may be reset under software control.

The actual program bit loading will occur one-half TC clock period after the falling edge of TSO for the first frame having Ap=0 that follows a series of frames with Ap=1. However, because of the possibility of a glitch on PTC and/or PRC, the DSP56401 may not receive the next frame of data correctly. For example, the host device (typically a digital signal processor) and the DSP56401 may see a different number of clocks as a result of the possible glitch. As mentioned above, the DSP56401 will recover by the next frame sync, but during this one frame, a 1 may appear in the Ap bit position. To avoid erroneous loading of program bits, Ap is ignored for one frame after a program word is loaded. This means Ap is ignored in the frame after the frame in which Ap=0 causes a program bit load. As a further protection against erroneous program bit loading, an isolated frame having Ap=1 can never cause program word loading.

7.1.1 Receiver Operation During PLL Locking

Once the proper program bits have been loaded, the receiver and PLL may lock to a valid AES/EBU or CP340 signal on one of the digital audio inputs, AIN0, AIN1, or AIN2. During locking, RBS occurrences may be further apart than 192 frame syncs and the DSP56401 status bits may not be sent 192 frames after the previous RBS. The user should determine the effect of these possibilities on his system and ensure that the system is stable and can return to proper operation.

7.2 DSP56001 Asynchronous Transmit/Receive SSI Interface

This application provides independent transmit and receive operation with asynchronous sample rates using a DSP56001 SSI port. The DSP56001 can perform transmit only, receive only, synchronous transmit/receive or asynchronous transmit/receive (sample rate conversion) functions. DSP56401 mode 0 selects three 24 bit time slots (channel A audio sample, channel B audio sample and non-audio data) per frame sync using SSI network mode. Transmit and receive block sync signals use the DSP56001's external interrupt inputs (edge-triggered mode). The LOCK signal is sensed by a Port B I/O pin. Figure 7-2 shows the interface signal connections.

7.3 DSP56001 Synchronous Transmit/Receive SSI and SCI Interface

This application provides independent transmit and receive operation at the same sample rate using a DSP56001 SSI port for audio samples and a SCI port for non-audio data. The DSP56001 can perform transmit only, receive only or synchronous transmit/receive functions. Real-time sample rate conversion is not possible with synchronous operation. DSP56401 mode 1 selects two 24 bit time slots (channel A and channel B audio samples) per frame sync using SSI network mode. Non-audio data is transferred using SCI shift register mode. In this example, the receive block sync and lock indicator signals use the DSP56001's SSI input flags. The transmit block sync is not needed since the user can issue a transmit modulator block reset command to reset the start of a block. Figure 7-3 shows the interface signals.

When the DSP56001 SCI is used for non-audio data transfer, the SCI transmitter enable (TE) and receiver enable (RE) bits in the SCI Control register must be enabled when the gated clock (RNS) is not

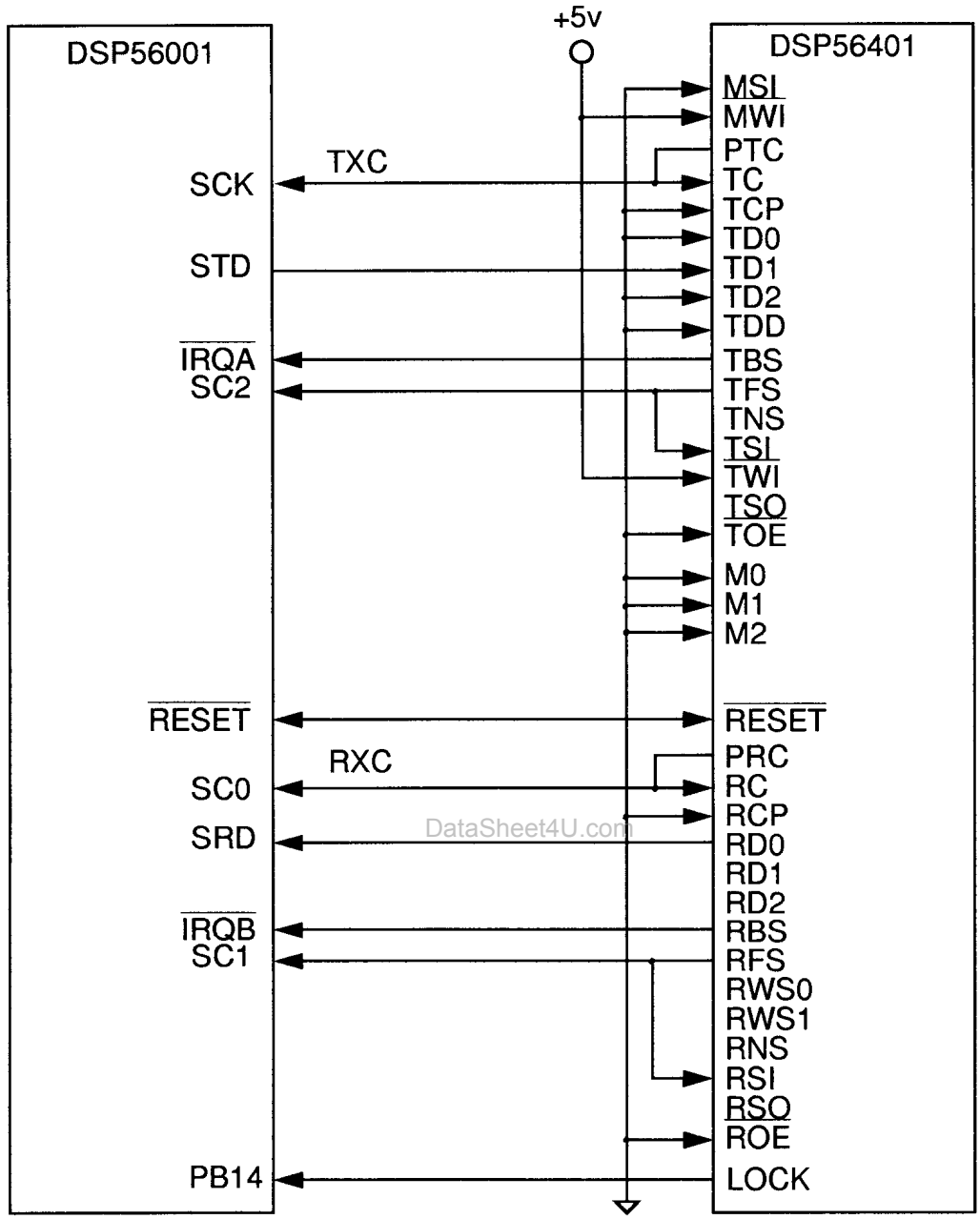


Figure 7-2 DSP56001 Asynchronous Transmit/Receive Interface

clocking. This can be accomplished by reading the port C data register to look for a RBS or RFS transition. The DSP56001 can read port C even if the port C pin is designated as a peripheral pin, as is the case for SC2. When a RBS or RFS transition occurs, the SCI should be enabled before the first RNS pulse occurs. Once enabled, the SCI will be synchronized to RBS or RFS unless a transmitter underrun or receiver overrun occurs.

Since this application uses only SSI and SCI pins, it is compatible with the DB15 "DSP port" connector on the NeXT computer and other compatible

products. The pinout of the NEXT "DSP port" is shown below:

1	SCK	9	GND
2	SRD	10	GND
3	STD	11	GND
4	SCLK	12	SC2
5	RXD	13	SC1
6	TXD	14	SC0
7	+12V, 500mA	15	GND
8	-12V, 100 mA		

7.4 DSP56156 Synchronous Transmit/Receive SSI Interface

This application provides independent transmit and receive operation at the same sample rate using a DSP56156 SSI port in its synchronous, external clock mode. The DSP56156 can perform transmit only, receive only or synchronous transmit/receive functions. Real-time sample rate conversion is not possible using one DSP56156 SSI because it has only one serial clock signal. However, asynchronous transmit/receive operation (such as in sample rate conversion) is possible with one DSP56156 by using one SSI for transmit and another SSI for receive (not shown). DSP56401 mode 4 selects three 16 bit time slots (channel A audio sample, channel B audio sample and non-audio data) per frame sync using SSI network mode. In this example, the receive block sync (RBS) signal uses the DSP56156's SSI input flag. Loss of lock indication is sensed by the DSP56156's edge-triggered interrupt input ($\overline{IRQA}$). Since the $\overline{IRQA}$ input is used as a DSP56156 mode select input during $\overline{RESET}$, LOCK is high impedance during $\overline{RESET}$. A pullup or pulldown resister should be used to set the DSP56156 mode. Figure 7-4 shows the interface signal connections.

The same DSP56156 interface can also support 24 bit audio sample transfer using DSP56401 mode 2. This mode provides four 16 bit time slots (16 MSBs of channel A audio sample, 8 LSBs of channel A audio sample with non-audio data byte, 16 MSBs of channel B audio sample and 8 LSBs of channel B audio sample followed by eight reserved bits) per frame sync using SSI network mode. The DSP must separate the non-audio data from the channel A sample and process the audio samples with double precision arithmetic.

7.5 Multiple DSP56401 SSI Interface

Multiple DSP56401 systems typically communicate via a shared serial digital audio bus. To the DSP56001 or DSP56156, this bus appears as a SSI port having multiple time slots in SSI network mode. The DSP56401 contains on-chip support for daisy-chaining time slots across multiple devices and for synchronizing multiple digital audio modulators and demodulators.

Figure 7-5 shows the DSP56401 attached to a digital audio system bus. This example has independent transmit and receive bus signals which support different transmit and receive sample rates simultaneously. The bus signals interface to previous time slots (if any) and to following time slots (if any). The adjacent time slots may be other DSP56401s, A/D converters, D/A converters or other serial devices. A DSP56001 may simultaneously communicate with any of these devices using the asynchronous interface described in Section 7.2. Figure 7-5 shows DSP56401 mode 0 but any "fast" mode (0, 2, 4, or 6) may be used for asynchronous transmit and receive operation.

System synchronization is an important issue which needs special attention. A single digital audio receive bus can only support one receive sample frequency at a time. Thus all receive bus timing signals must be supplied by one DSP56401 which is locked to a digital audio bit stream. The source of the receive bus timing signals is called the "receive clock master" and is selected by asserting the DSP56401 $\overline{ROE}$ input. All non-master demodulators are called "receive slaves" and obey the timing signals of the master receiver. Only one $\overline{ROE}$ should be asserted per digital audio bus. The DSP typically looks at the status bits or LOCK signal of each DSP56401 to determine which device should be the receive bus master.

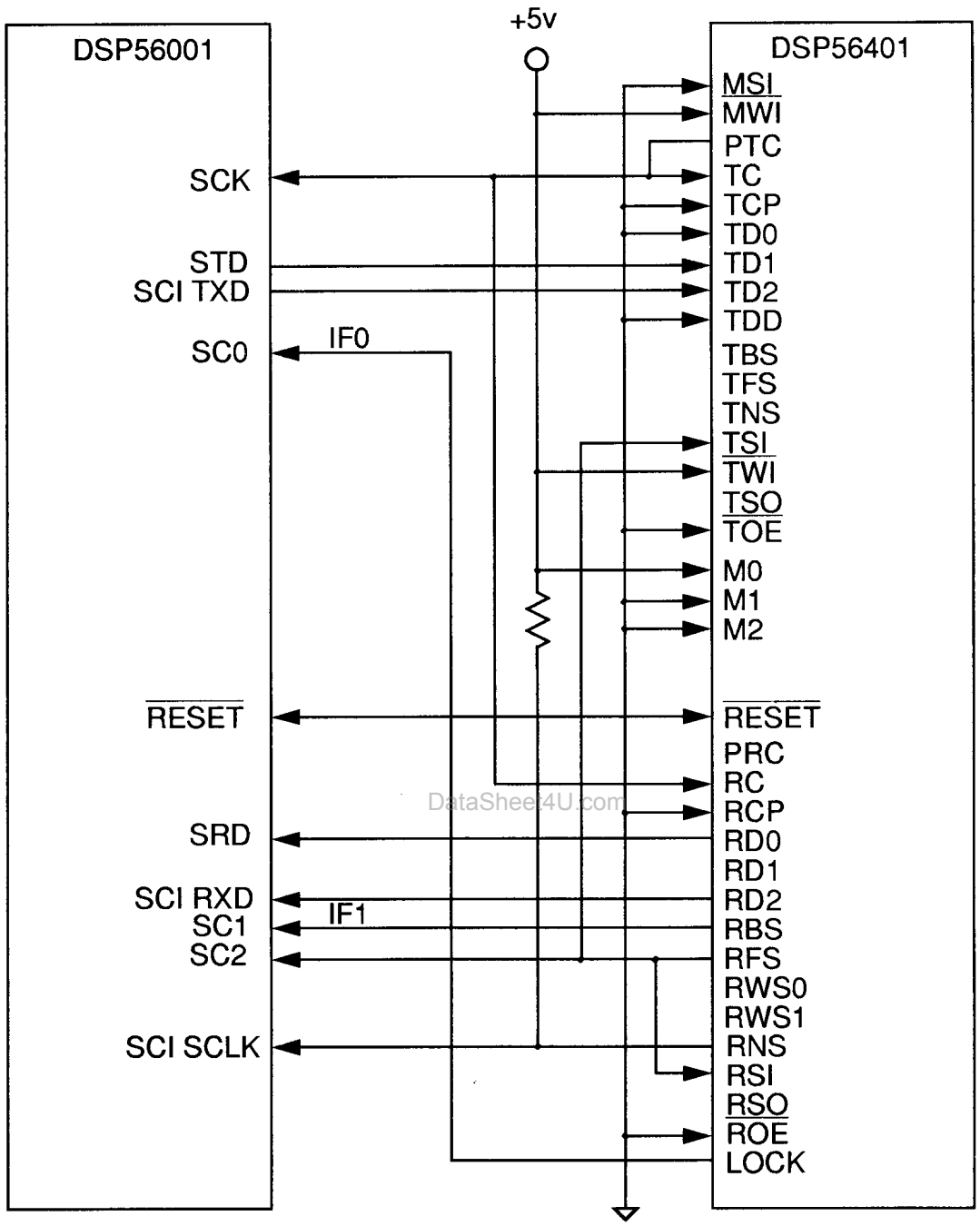


Figure 7-3 DSP56001 Synchronous Transmit/Receive Interface

The digital audio transmit bus can also support only one transmit sample frequency at a time. Thus all transmit bus timing signals must be supplied by one DSP56401 modulator which is clocked by a crystal oscillator, its own demodulator or another DSP56401 demodulator. The source of the transmit bus timing signals is called the "transmit clock master" and is selected by asserting the DSP56401 $\overline{\text{TOE}}$ input. All non-master modulators are called "transmit slaves" and obey the timing signals of the

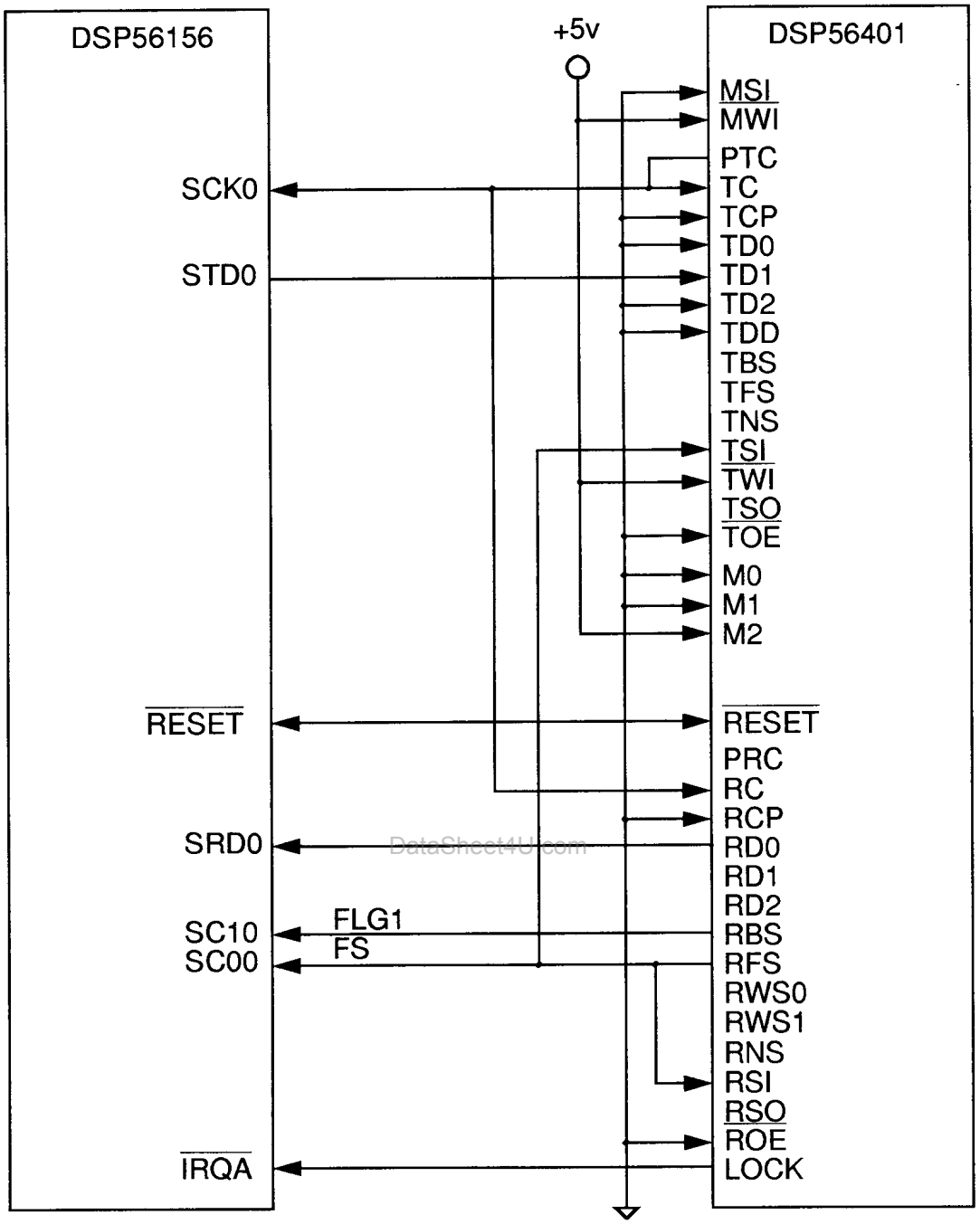


Figure 7-4 DSP56156 Synchronous Transmit/Receive Interface

master transmitter. Only one $\overline{TOE}$ should be asserted per digital audio bus. The DSP typically selects the transmit master to be the same as the receive master in synchronous situations and different in asynchronous situations.

Multiple receive demodulators cannot be synchronized together unless the digital audio sources are also synchronized together. In general, cable effects and pin delays make this a difficult task due to margin loss. The DSP56401 has no explicit demodulator synchronization signals.

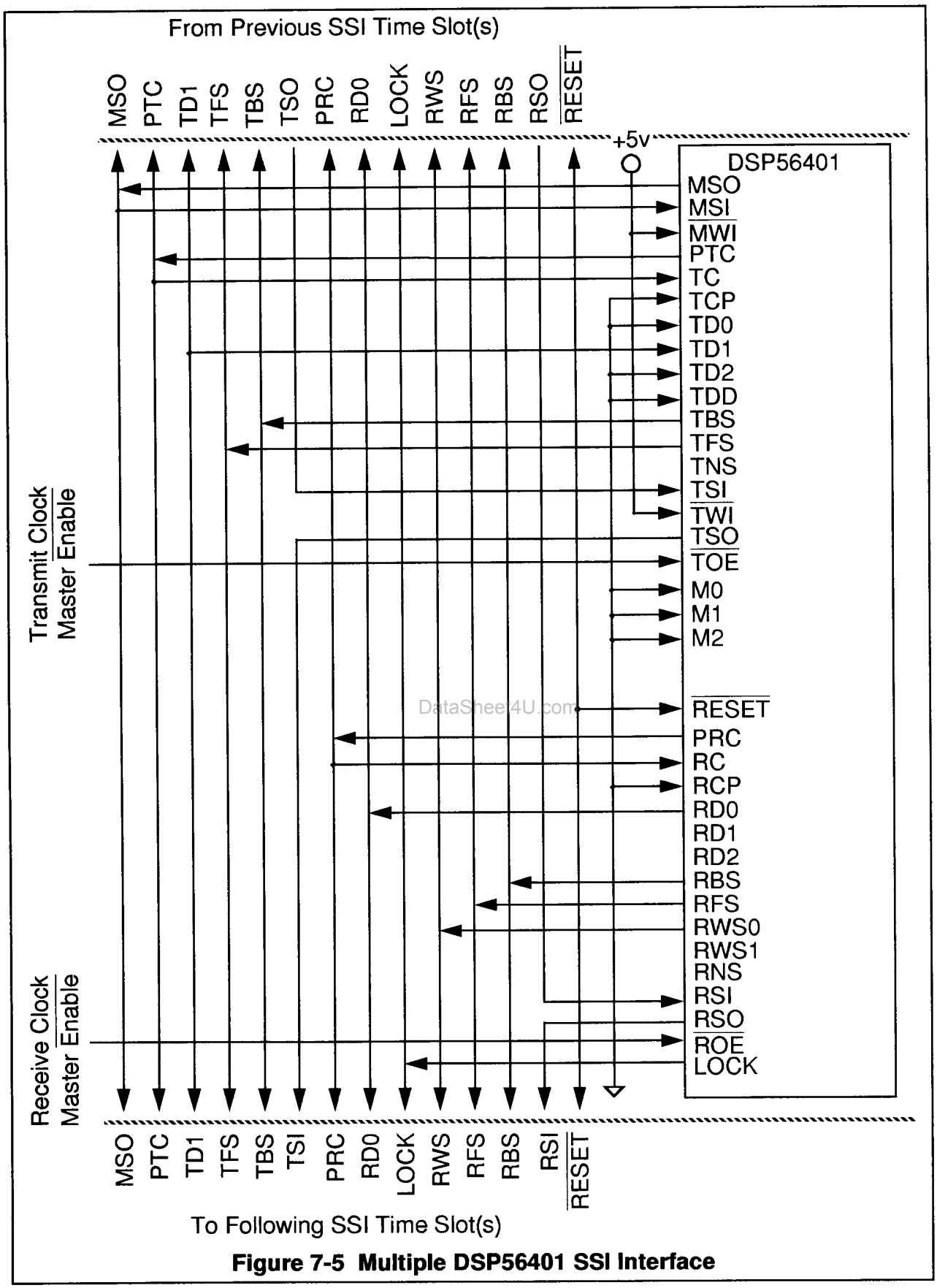


Figure 7-5 Multiple DSP56401 SSI Interface

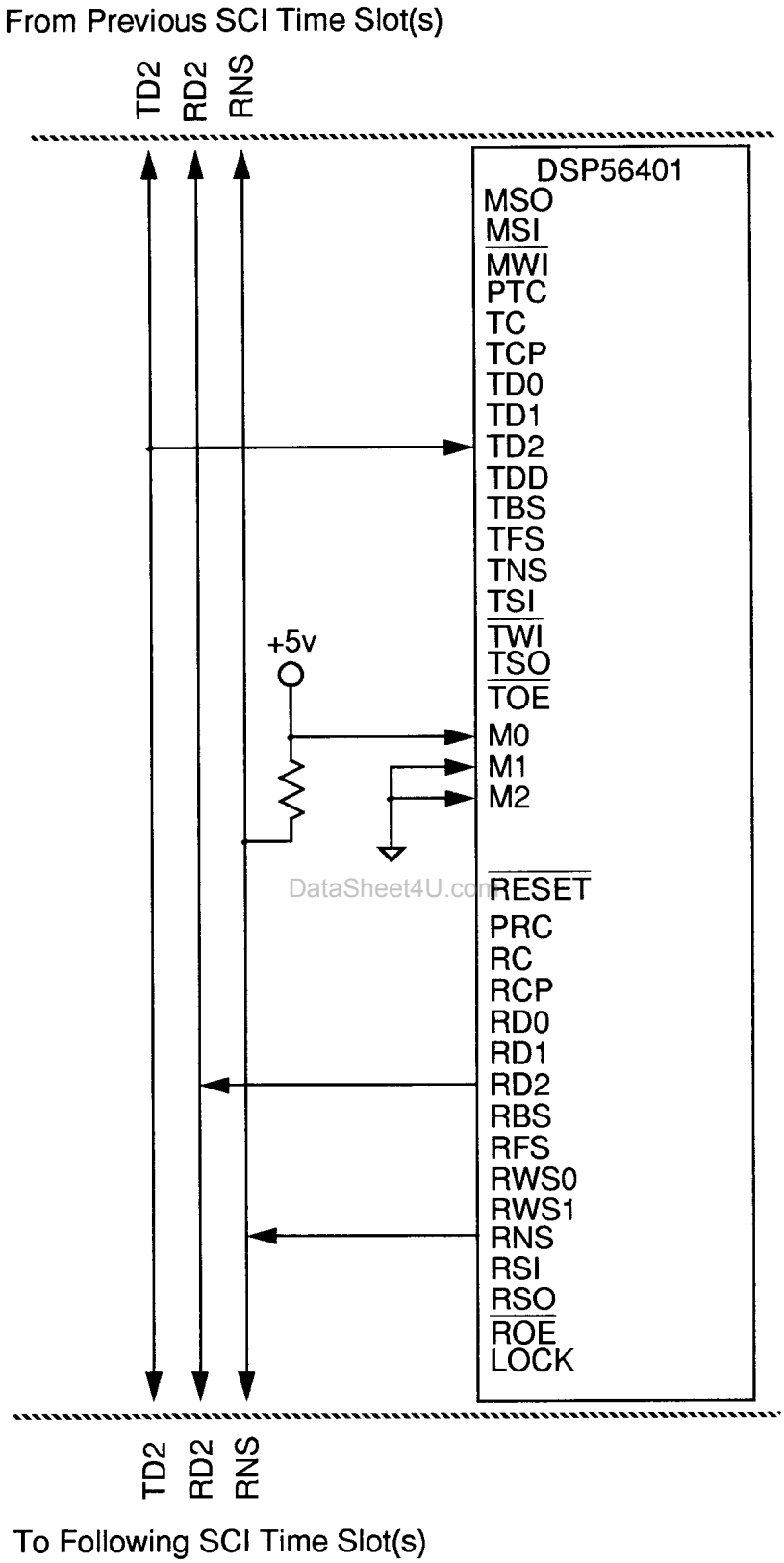


Figure 7-6 Multiple DSP56401 SCI Interface

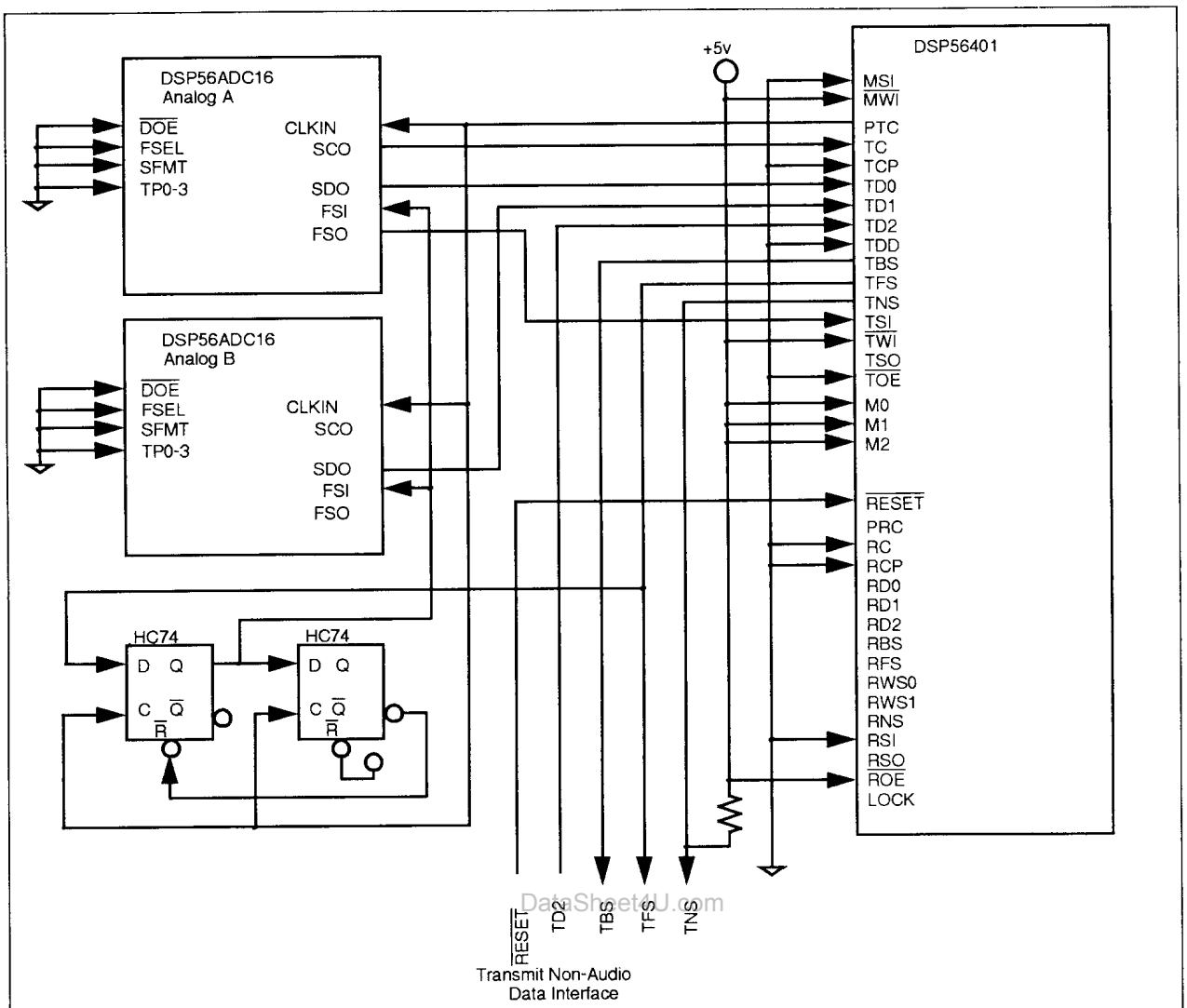


Figure 7-7 Stereo DSP56ADC16 Digital Audio Microphone

However, a master demodulator can provide its PLL clock to a slave demodulator by connecting the master's PRC output to the slave's OSCIN input. Then each demodulator is a free running state machine responsive to the digital audio sync patterns (preambles).

Multiple transmit modulators can be synchronized together using the modulator sync out (MSO) and modulator sync in (MSI) signals. All modulators must also use a common clock source for synchronization of modulators. The transmit master provides MSO and all slave DSP56401s synchronize to it via MSI. Thus all modulators in the system are synchronized together and transmit their preambles at the same time.

The number of DSP56401s per digital audio bus is primarily limited by the maximum SSI, TC or RC serial clock rates. Capacitive loading on the data and sync signals is the secondary limit. The serial clock rates can be minimized by selecting serial modes having low bit counts per frame. In synchronous applications, slow non-audio modes can be used to reduce the bit count per frame.

7.6 Multiple DSP56401 SCI Interface

Multiple DSP56401 systems typically communicate via a shared serial digital audio bus. As discussed in Section 7.5, an SSI port having multiple time slots in SSI network mode can be used to implement a

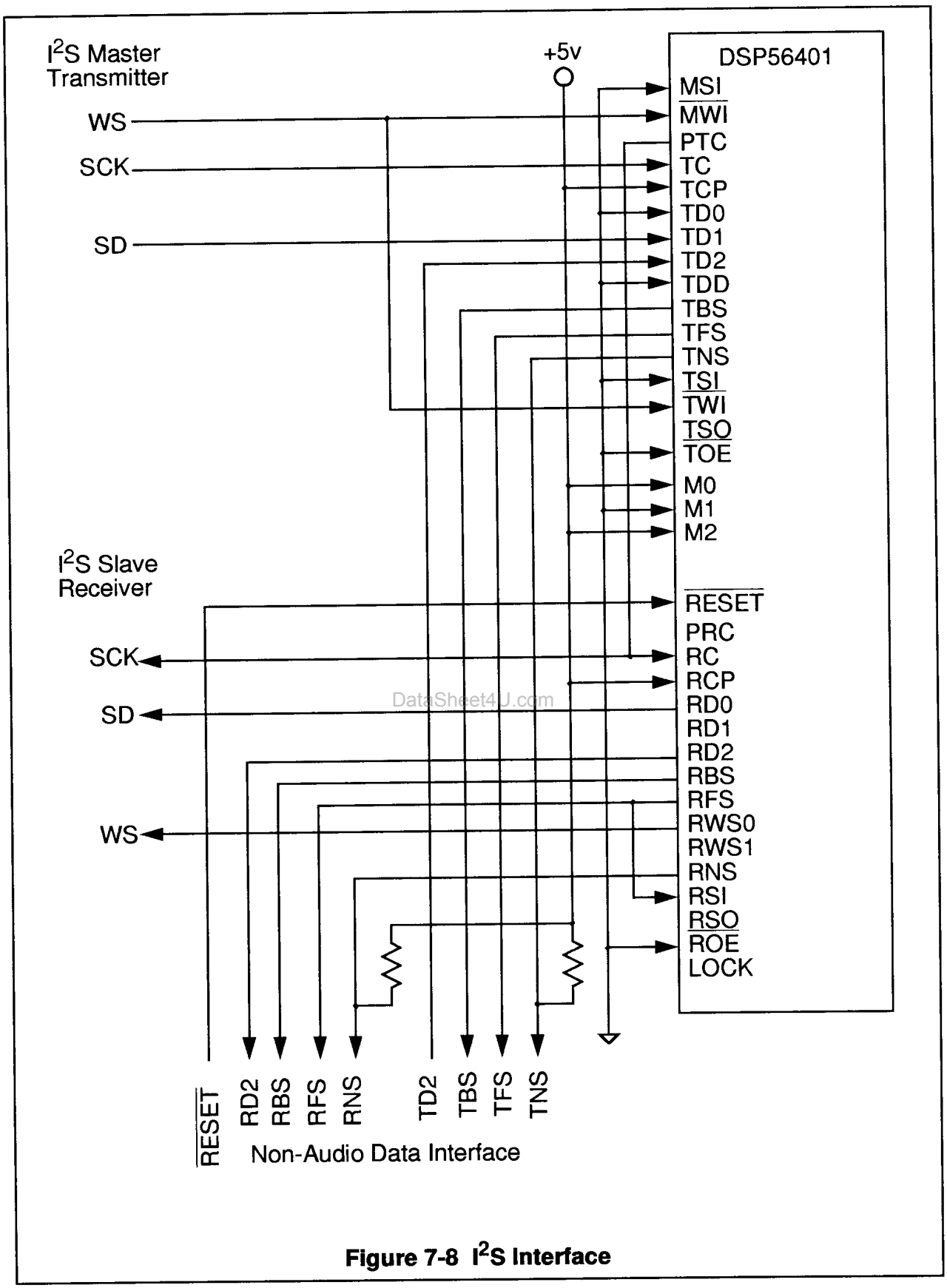


Figure 7-8 I2S Interface

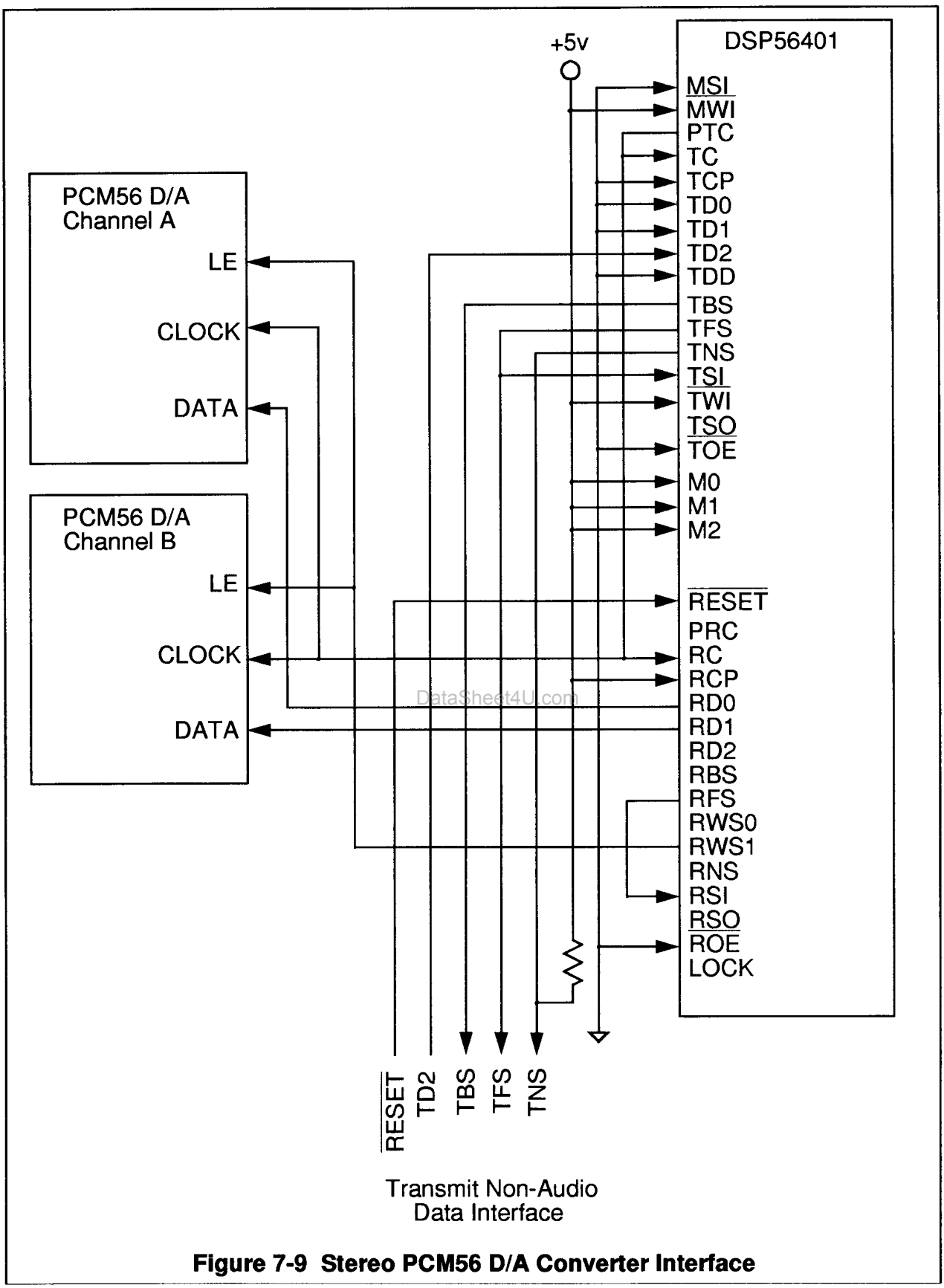


Figure 7-9 Stereo PCM56 D/A Converter Interface

digital audio system bus. This section shows how to augment this digital audio system bus with a separate non-audio data bus using a DSP56001 SCI port in shift register mode. Note that the SCI shift register mode is limited to synchronous transmit/receive operation.

Figure 7-6 shows the additional DSP56401 signal connections to add a non-audio data bus to Figure 7-5. The bus signals interface to previous time slots (if any) and to following time slots (if any). The adjacent time slots may be other DSP56401s, A/D converters, D/A converters or other serial devices. A DSP56001 may simultaneously communicate with any of these devices using the synchronous interface described in Section 7.3. Figure 7-6 shows DSP56401 mode 1 but any "slow" mode (1, 3, 5 or 7) may be used.

System synchronization is an important issue which needs special attention. A synchronous non-audio data bus can only support one sample frequency at a time. The non-audio data is clocked by TNS or RNS which are gated clocks derived from TC or RC respectively. Thus PTC and PRC in Figure 7-5 should be identical or only one serial clock should be used. All non-audio data bus timing signals must be supplied by one DSP56401 which is either locked to a digital audio bit stream or clocked by a crystal oscillator. The source of the bus timing signals is called the "clock master" and is selected by asserting the DSP56401 $\overline{\text{ROE}}$ (for RNS) or $\overline{\text{TOE}}$ (for TNS) input. All non-master DSP56401s are called "clock slaves" and obey the timing signals of the clock master. Only one $\overline{\text{ROE}}$ or $\overline{\text{TOE}}$ should be asserted per digital audio bus. The DSP typically looks at the status bits or LOCK signal of each DSP56401 to determine which device should be the clock master.

The number of DSP56401s per non-audio data bus is primarily limited by the maximum SCI, TNS or RNS serial clock rates. Capacitive loading on the data and sync signals is the secondary limit. The pullup resistor does not limit the speed since TNS or RNS is driven high before going high impedance. Note that only one TNS or RNS resistor is needed per system.

7.7 Stereo DSP56ADC16 Digital Audio Microphone

This application demonstrates a stand-alone, stereo microphone with a digital audio output. The microphone uses Sigma-Delta A/D converters and transmit only DSP56401 operation. Two DSP56ADC16s provide simultaneously sampled, stereo A/D conversion. The DSP56ADC16 provides 32 SCO clocks per frame sync (FSO) but only uses the first 16 clocks for the audio sample. DSP56401 mode 7 selects one 16 bit time slot using three pins (digital A audio sample, digital B audio sample and non-audio data). Even though there is only one 16 bit time slot, at least 32 clocks per frame sync are required to load the non-audio data. Figure 7-7 shows the interface signal connections.

Sample synchronization is an important system design issue. The A/D sample frequency is determined by the DSP56ADC16 clock input (CLKIN), which is 128 times the sample frequency. CLKIN is driven by the DSP56401's programmable clock output (PTC), optionally divided down from one of the four on-chip oscillators. The oscillator selection and divide ratio are controlled by the program word loaded into the non-audio data port. The transmit modulator is driven by the same crystal oscillator divided down to 64 times the sample frequency. The DSP56ADC16 divides CLKIN by 4 to form the SCO serial bit clock. The transmit modulator state machine generates a transmit frame sync (TFS) each sample period. Since it is connected to the DSP56ADC16 frame sync input (FSI), TFS defines the A/D conversion time for simultaneous stereo sampling.

7.8 I^2S Interface

The I^2S interface is an inter-IC serial bus for transfer of two channel digital audio samples. The hardware interface provides serial data (SD), word select (WS) and serial clock (SCK) lines. The serial data is organized as a left channel sample followed by a right channel sample, MSB first. The audio samples may be any word size but are typically 16 bits each.

This application provides a digital audio modulator slaved to an I^2S master transmitter and a digital audio demodulator configured as an master transmitter to an I^2S slave receiver. The application example shown in Figure 7-8 uses DSP56401 mode 5 to select 16 bit audio samples. If 24 bit audio samples are desired, DSP56401 mode 1 can be used.

The digital audio modulator is synchronized to the I^2S master's word select and serial clock. Since the modulator state machine requires a minimum of 64 clocks per sample period, the I^2S master should provide at least 64 clocks per word select period. The I^2S word select synchronizes the transmit serial interface via the transmit word sync input ($\overline{TWI}$) and the transmit modulator via the modulator word sync input ($\overline{MWI}$).

The digital audio demodulator recovers a serial bit clock and word select from the digital audio bit stream. Thus the demodulator is inherently a master timing generator. The receive serial interface control signals can directly drive an I^2S slave receiver.

The non-audio data port is available to transmit and receive channel status or user bits information via TD2 or RD2. Note that the program word must be loaded to configure DSP56401 for the desired serial mode and clock generation. After that, the program and status words can be ignored.

7.9 Stand-alone Burr-Brown PCM56 D/A Interface

This application demonstrates a stand-alone, stereo D/A interface using the Burr-Brown PCM56. It also applies to many Japanese digital audio interfaces (which may require TDD=1). This example does not include an oversampling digital filter, so analog anti-aliasing filters are required. The PCM56 uses a simple serial protocol having a serial data input (DATA), a latch enable (LE) and a serial data clock (CLOCK). DSP56401 mode 7 selects one 16 bit time slot across three pins (channel A audio sample, channel B audio sample and non-audio data). Even though there is only one 16 bit time slot, at least 32 clocks per frame sync are required to transfer the non-audio data. Figure 7-9 shows the interface signals.

Sample synchronization is an important system design issue. The receive demodulator PLL recovers a serial clock, frame sync and block sync from the digital audio bit stream. The D/A serial data CLOCK is driven by the DSP56401's programmable clock output (PTC), optionally divided down from the on-chip PLL oscillator. The oscillator selection and divide ratio are controlled by the program word loaded into the non-audio data port. PTC also drives the receive serial interface clock (RC). The D/A sample frequency is determined by DSP56401's receive word sync (RWS1) which controls the D/A latch enable. Since both LEs are driven by the same signal, the D/As simultaneously output analog signals (phase-coherent stereo).

More recent D/A converters (such as the PCM58) offer 18-20 bit word sizes. DSP56401 mode 3 can be used to support up to 24 bit word sizes. In this case, the RWS1 signal is several RC clocks later than needed by the D/A converter latch enable (LE). One simple solution is to delay the serial data inputs (DATA) several RC clocks using two HC164 shift registers (not shown). RD0 and RD1 delayed by 6 RC clocks correctly aligns with LE for the 18 bit PCM58. RD0 and RD1 delayed by 4 RC clocks provides the correct LE alignment for a 20 bit D/A converter.

7.10 EPROM-Based Non-Audio Data Loading

This application demonstrates how non-audio data may be loaded from an EPROM using DSP56401 modes 1, 3, 5 and 7. The hardware is shown in Figure 7-10. An EPROM supplies 192 x 8 = 1536 bits of non-audio information, repeated each block. A binary counter increments the EPROM address to select the proper non-audio bit. In this example, the first non-audio bit is at binary address 1. User options (such as sample rate selection, preemphasis and source number, etc.) may be selected by changing the EPROM address range or

Table 7-1 48 kHz Example

TC Clocks Per 48 kHz Frame Rate	TNS Low to TD2 Valid For Serial Mode 1 (ns)	TNS Low to TD2 Valid For Serial Modes 3,5,7 (ns)
32	1232	581
64	581	255
128	255	92
256	92	11

the data output bit with switches, jumpers or software-controlled muxes or output pins. Sample address codes or time of day codes are not supported by this example.

The primary design consideration is the delay from the TNS falling edge to TD2 valid. The counter $\overline{CLK}$ to Q delay plus the EPROM address access time plus the TD2 setup time plus the TNS delay from TC must be less than the TNS low width. The equation shown below gives the allowable TNS falling edge to TD2 valid delay for any given sample frequency, and Table 7-1 gives an example at 48 kHz showing the time available for the sum of counter and EPROM access timings.

The HC4040 binary ripple counter is rather slow ($\overline{CLK}$ to Q11 is 363 ns at 85 C). For slower TC rates, the HC4040 ripple counter is fast enough for reasonable EPROM access times. At faster TC rates, a synchronous counter should be substituted for the HC4040 and/or the EPROM data output should be pipelined through a HC74 flip-flop clocked by $\overline{TNS}$ to relax the required EPROM access time (not shown). If the data is pipelined, the first non-audio bit is at binary address 0.

$$(\tau_{CLKtoQ} + \tau_{AddressValidtoOUTPUT} + \tau_{TD2setup} + \tau_{TCtoTNS}) < (TNS_{Low}Period)$$

where $TNS_{Low}Period$ = 2 TC periods for mode 1
= 1 TC period for modes 3, 5, and 7

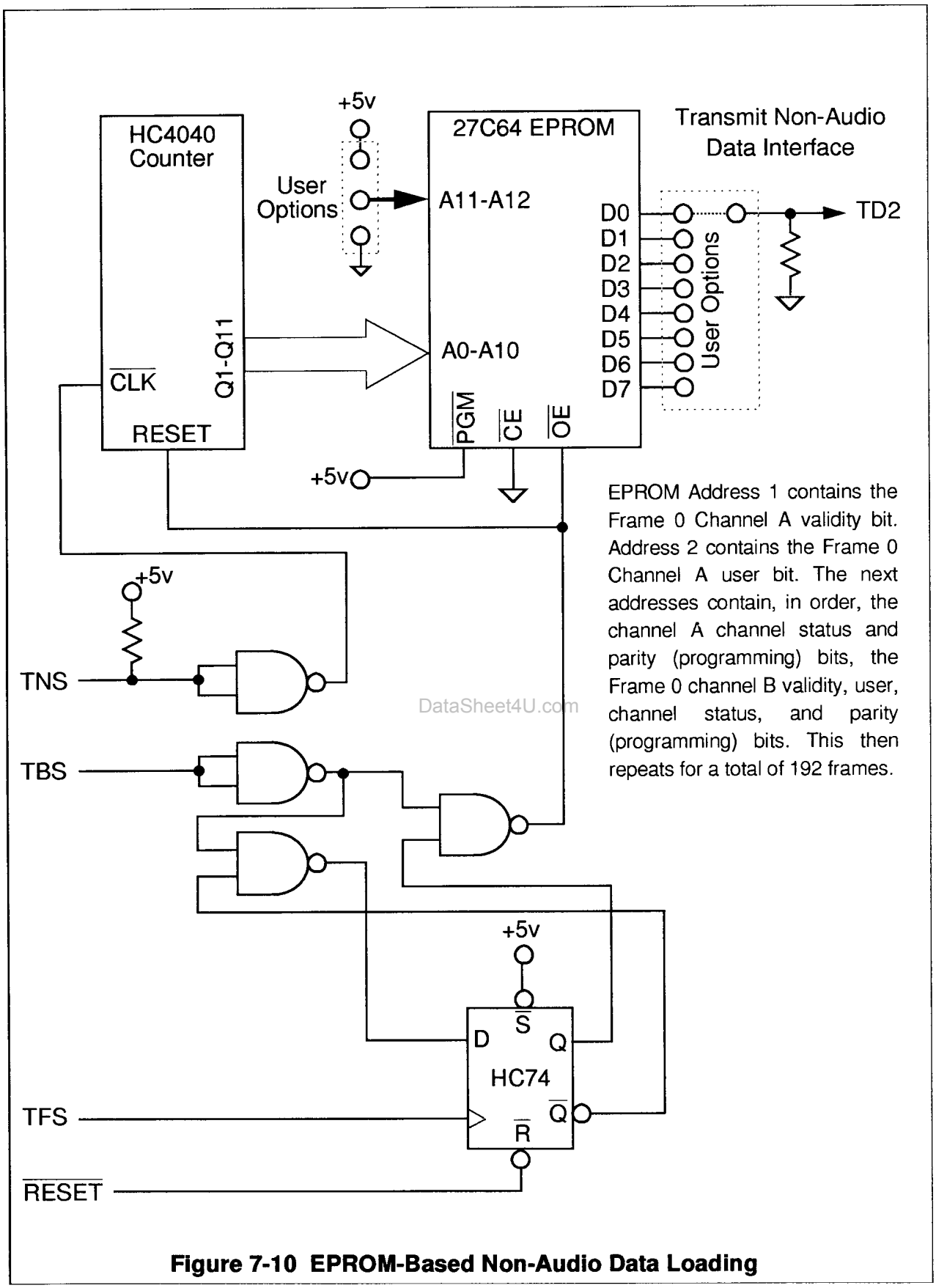


Figure 7-10 EPROM-Based Non-Audio Data Loading

Analog Applications Hardware

8.1 Modulation Interfaces

The modulated digital audio data uses one of three transmission formats - balanced electrical, unbalanced electrical and fiber optic. The modulation interfaces provide isolation, device protection, drive conversion and level conversion between the DSP56401 and the transmission media.

8.1.1 Balanced AES/EBU and CP340 Receiver

Balanced digital audio inputs are used in professional audio equipment. Figure 8-1 shows two receiver circuits using the MC34050 EIA-422/423 transceiver chip. The MC34050 acts as a differential comparator providing high common mode rejection, hysteresis and level translation. Both circuits use transformers for DC isolation and improved noise rejection. One circuit uses a 1:1 transformer, the other circuit uses a 1:3 step-up transformer for increased voltage swing with attenuated signals. In some applications the transformer may be eliminated, although this violates the EBU specification for isolation (the transformer is recommended but not required in the AES and CP340 specifications). The AES, EBU and CP340 (balanced electrical) specifications call for a 'nominally resistive' load over the range of 0.1 to 6 MHz. Typical LAN-type transformers usually have greater interwinding capacitance than allowed in the specification, particularly when multiplied by 3^2, but may work acceptably in a low-cost application. We have used both the BH Electronics 500-1770 LAN transformer and the Scientific Conversions SC-916-1 transformer, which is optimized for AES/EBU operation, with good success. We have not been able to thoroughly test either of these transformers, so are unable to make

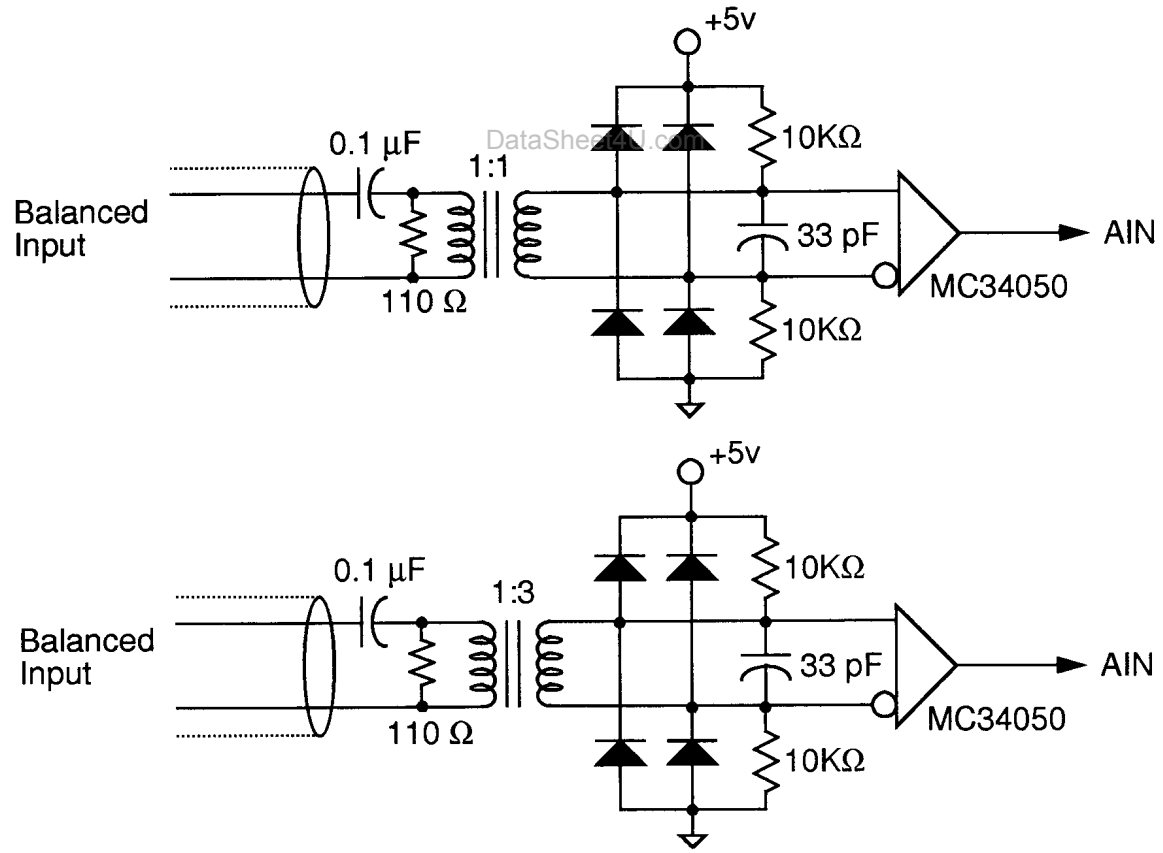


Figure 8-1 Balanced AES/EBU and CP340 Receivers

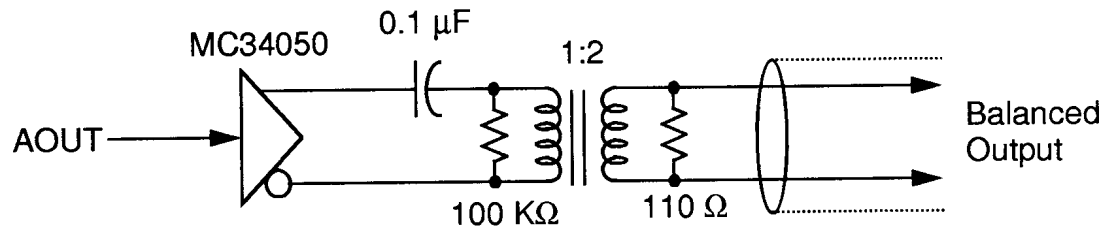


Figure 8-2 Balanced AES/EBU and CP340 Transmitter

a completely valid comparison or recommendation for a particular application. The AES, EBU and CP340 (balanced electrical) formats currently stipulate a three-pin XLR connector (IEC 268-12, 1975) with pin one grounded (polarity of the other two pins is unimportant), but other connectors may be allowed at a later date. The cable shield should be floated at the receiver and grounded at the transmitter.

8.1.2 Balanced AES-EBU and CP340 Transmitter

Balanced digital audio outputs are used in professional audio equipment. Figure 8-2 shows a transmitter circuit using the MC34050 EIA-422/423 transceiver chip. The MC34050 acts as a differential driver providing high current, short circuit protection and noise isolation from the DSP56401 PLL. This circuit uses a transformer (1:1 to 1:1.4 stepup for AES/EBU, 3:1 to 9:1 stepdown for CP340) for DC isolation and level conversion. In some applications the transformer may be eliminated, although this violates the EBU specification for isolation (the transformer is recommended but not required in the AES and CP340 specifications). We used both the BH Electronics 500-1770 LAN transformer and the Scientific Conversions SC-916-1 transformer, which is optimized for AES/EBU operation, with good success. We have not been able to thoroughly test either of these transformers, so are unable to make a completely valid comparison or recommendation for a particular application. The AES/EBU and CP340 formats currently stipulate a three-pin XLR connector (IEC 268-12, 1975) with pin one grounded (polarity of the other two pins is unimportant), but other connectors may be allowed at a later date. The cable shield should be grounded at the transmitter and floated at the receiver.

8.1.3 Unbalanced CP340 Receiver

Unbalanced digital audio inputs are used in consumer audio equipment. Figure 8-3 shows a receiver circuit using the MC34050 EIA-422/423 transceiver chip. The MC34050 acts as a differential comparator providing hysteresis and level translation. The circuit uses a 1:3 step-up

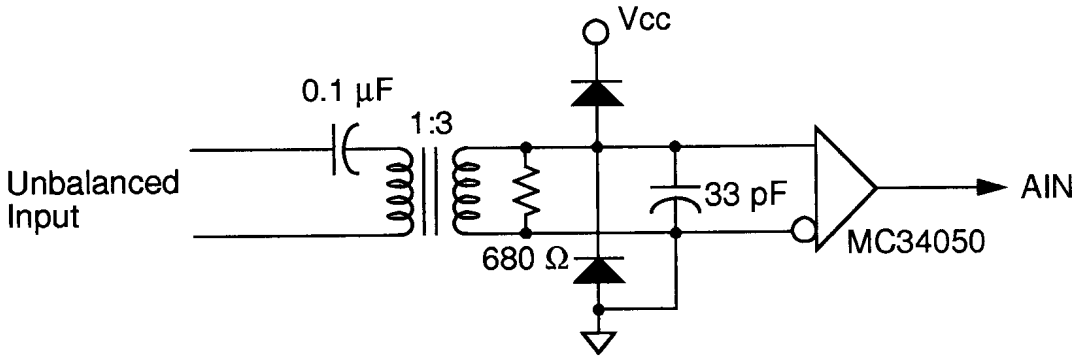


Figure 8-3 Unbalanced CP340 Receiver

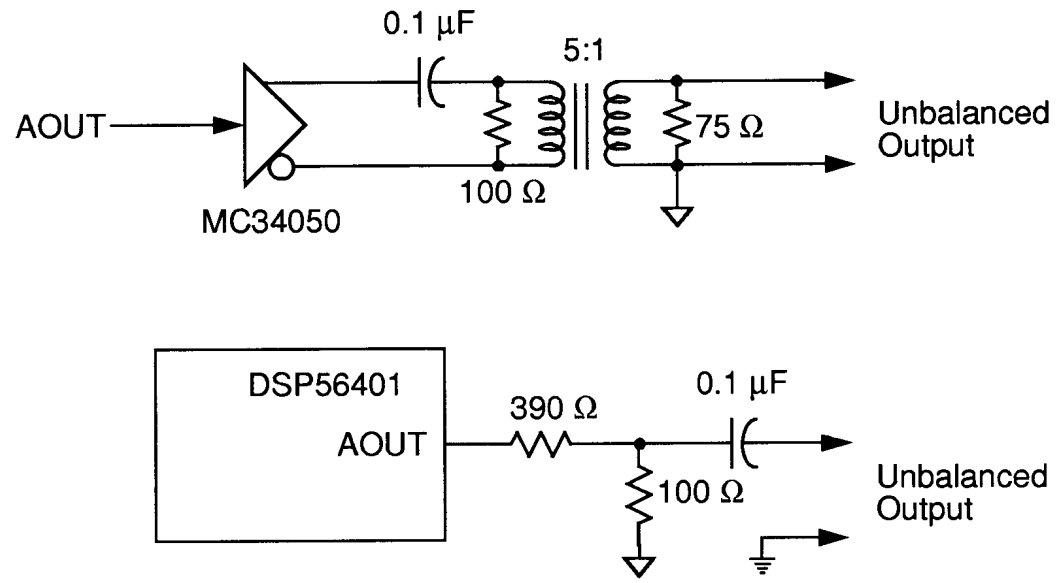


Figure 8-4 Unbalanced CP340 Transmitters

transformer for increased voltage swing with CP340 signals. In some applications the transformer may be eliminated, but since the MC34050 changes states at 0.4 volts differential input and the CP340 specification calls for a only a 0.5 volt signal amplitude at the source, this is not generally recommended. This format stipulates a phono-type connector (EIAJ RC-6703), sometimes called an RCA connector.

8.1.4 Unbalanced CP340 Transmitter

Unbalanced digital audio outputs are used in consumer audio equipment. Figure 8-4 shows two transmitter circuits. One circuit uses a MC34050 EIA-422/423 transceiver as a differential driver providing high current, short circuit protection and noise isolation from the DSP56401 PLL. The circuit uses a 5:1 step-down transformer for the decreased voltage swing specified by CP340 (0.5 volt

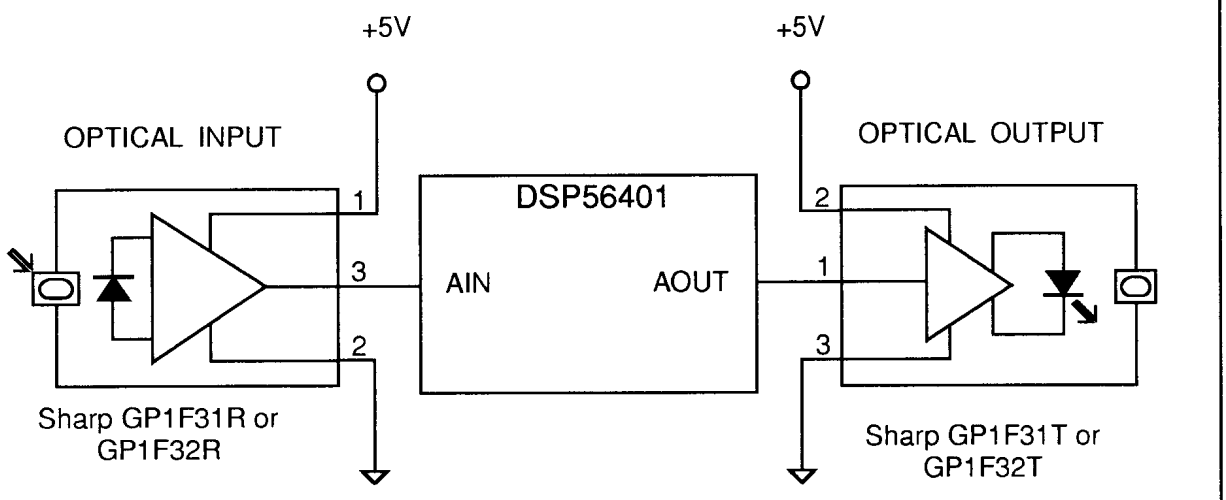


Figure 8-5 Fiber Optic CP340 Interface (Sharp)

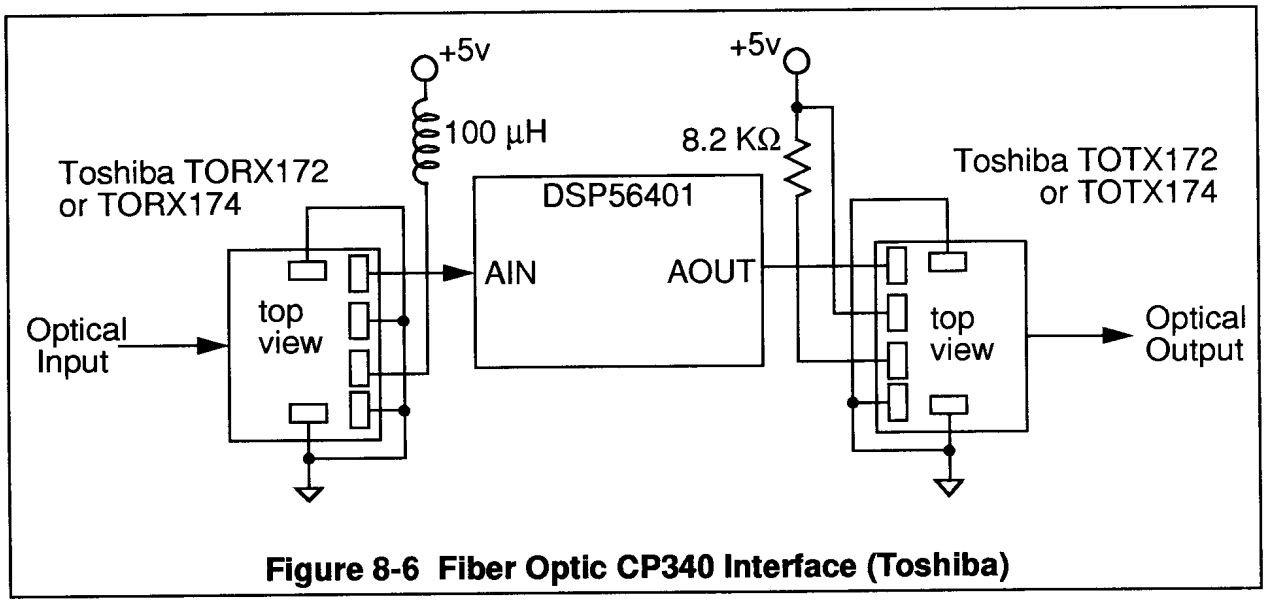


Figure 8-6 Fiber Optic CP340 Interface (Toshiba)

amplitude). The other circuit uses a simple resistor divider directly driven by the DSP56401 AOUT pin and may be sufficient for short transmission distances. Note that this circuit does not satisfy the CP340 impedance requirements. This format stipulates a phono-type connector (EIAJ RC-6703), sometimes called an RCA connector.

8.1.5 Fiber Optic CP340 Interface

This application uses a fiber optic module designed for digital audio communications. The DSP56401 directly interfaces to each module as shown in Figure 8-5 and Figure 8-6. Figure 8-5 shows a Sharp fiber optic module and Figure 8-6 shows a Toshiba fiber optic module. This format stipulates an optical connector (EIAJ RCZ-6901) and light wavelength (660 nm ± 30 nm), and both of these device families feature integral fiber-optic connectors and drivers/detectors of the correct type.

8.2 Oscillator Circuits

The DSP56401 provides four general purpose, on-chip oscillator inverters which may be used as fixed frequency oscillators or voltage-controlled oscillators (VCOs). Alternatively, an external clock signal may be input via an oscillator pin. Each oscillator circuit may be internally selected and/or frequency-modified (divided down or doubled) under software control. A clock generation block diagram is shown in Figure 2-6 and Figure 2-7. This section describes the external analog components required to implement various oscillator circuits.

The transmit modulator requires a fixed frequency oscillator having a minimum clock frequency of 64 times the sample rate. In a transmit only situation, up to three oscillators may be required to cover 48, 44.1 and 32 kHz sample rates. However, one 12.288 MHz oscillator can cover both 48 and 32 kHz sample frequencies if the internal divide by 1.5 circuit is used. Typical applications use two oscillators for transmit functions.

The receive demodulator requires a voltage controlled oscillator having a minimum clock frequency of 512 times the receive sample frequency. In a receive only situation, up to three oscillators may be required to cover 48, 44.1 and 32 kHz sample rates. However, one 12.288 MHz voltage controlled LC oscillator can cover both of the 44.1 and 48 kHz sample rates, and one 24.576 MHz voltage controlled LC oscillator can cover all three of the 44.1, 48 and 32 kHz sample rates if the internal divide by 1.5 circuit is used. Typical applications use one oscillator for receive PLL functions.

An internal frequency doubler also allows an external VCO having a frequency of 256 times the receive sample frequency to be used. Internal dividers allow a maximum clock frequency up to 1024 times the sample frequency in some

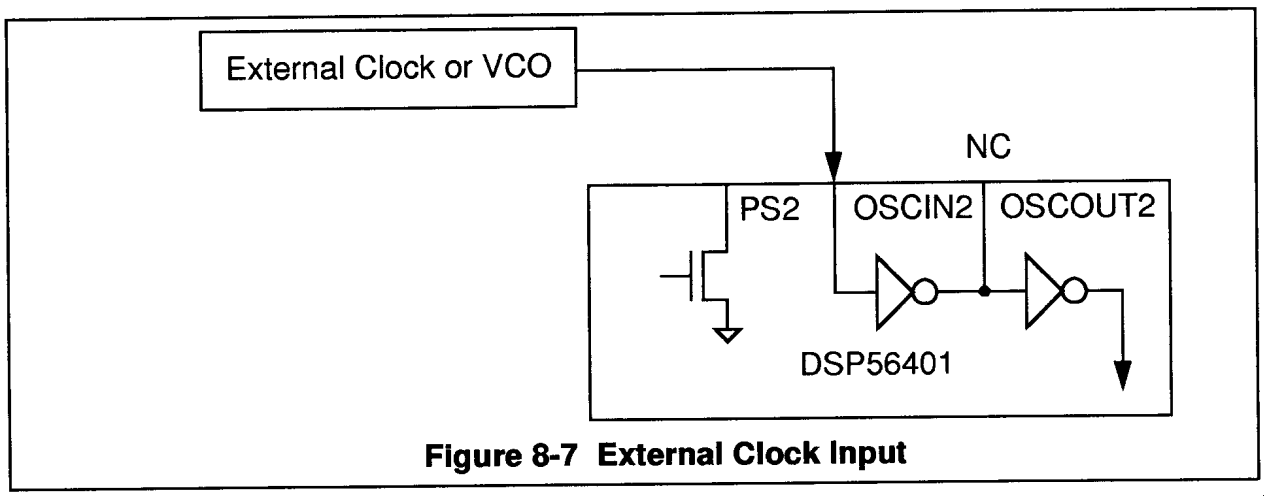


Figure 8-7 External Clock Input

applications. The minimum input frequency is determined by the internal state machines and the maximum input frequency is constrained by the electrical timing characteristics.

8.2.1 External Clock Input

An external clock may be input via any OSCINx pin. This is useful when another device provides the DSP56401 system clocks. An example using oscillator 2 is shown in Figure 8-7. The external clock or VCO must provide CMOS input levels into OSCIN2. OSCOUT2 should not be connected and PS2 may then be used as a general purpose I/O pin to control external devices.

8.2.2 Fixed Crystal Oscillator

Fixed crystal oscillators may be used to define the sample frequency of the transmit modulator or external A/D converters. A parallel resonant crystal circuit is shown in Figure 8-8. This example, using oscillator 2, shows an 11.2896 MHz crystal which is 256 times the 44.1 kHz sample frequency. The oscillator is internally selected and divided down under software control. The oscillator may also be turned off using the programmable output PS2 to pull OSCIN2 to ground. This prevents clock beating which may occur if multiple oscillators are active at the same time.

8.2.3 Voltage Controlled LC Oscillator

The receive demodulator requires an external voltage controlled oscillator (VCO) responsive to the phase detector outputs PUP and PDOWN. The VCO range must cover the receive frequencies of interest. Figure 8-9 shows a LC VCO designed to operate over the frequency range of 10-14 MHz

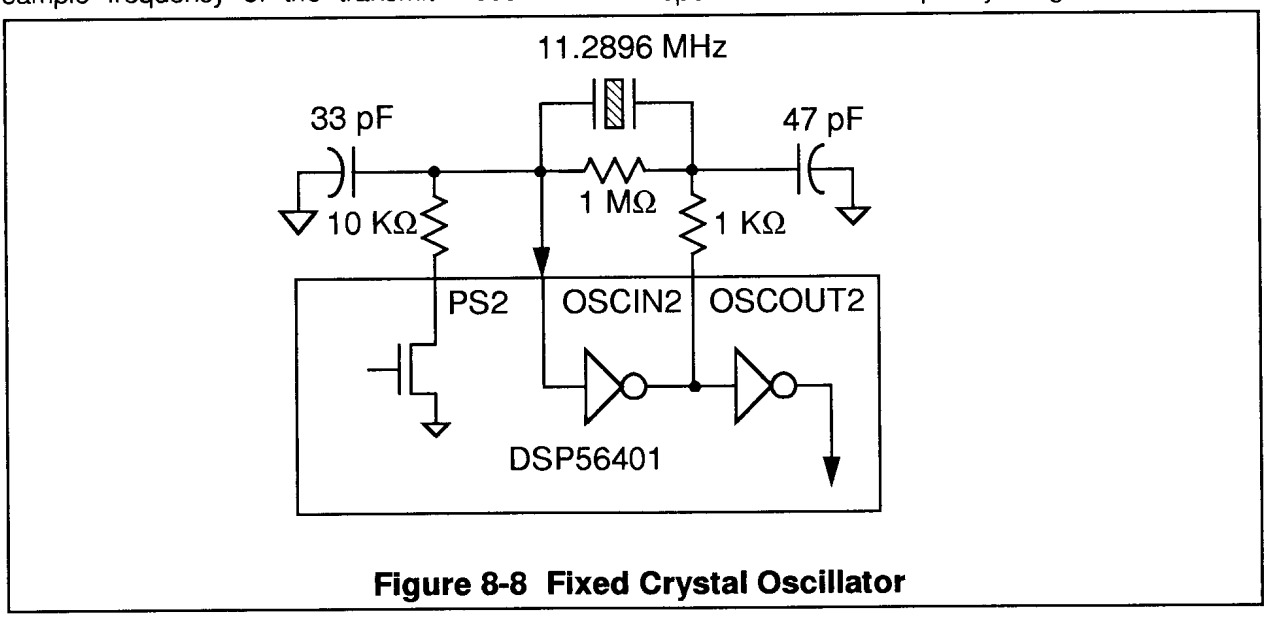


Figure 8-8 Fixed Crystal Oscillator

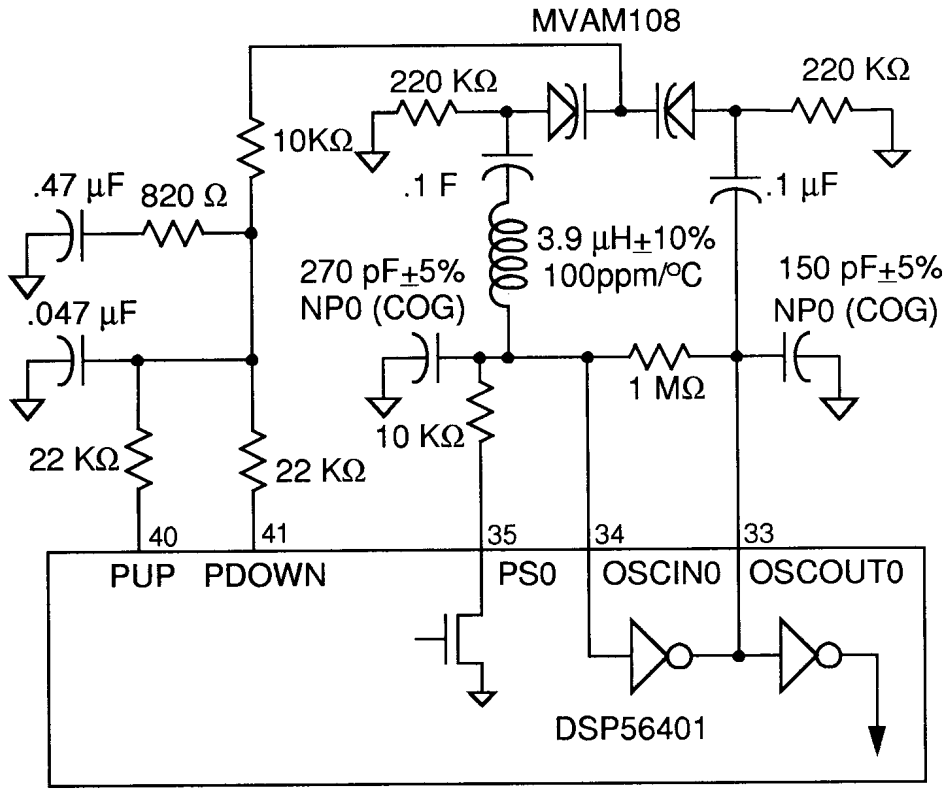


Figure 8-9 Voltage Controlled LC Oscillator (12 MHz)

using MVAM108 varactors, which enables recovering both 48 and 44.1 kHz sample rates. We recommend at least 30 degrees of phase margin which means at least a 820Ω damping resistor. Program bits should be set to P21=0 and P20=0 for positive phase detector polarity. Use good analog layout and maintain good analog ground planes for minimum jitter. The analog ground should be tied to VSSB and VSSI at the DSP56401.

Figure 8-10 shows an LC VCO designed to operate over the frequency range of 20-25 MHz using MV209 varactors which covers all three of the 44.1, 48 and the 32 kHz sample rates (using the divide by 1.5 option for 32 KHz only). We recommend at least 30 degrees of phase margin which means at least a 820Ω damping resistor. This circuit uses an inverting loop filter, so program bits should be set to P21=0 and P20=1. Use good analog layout and maintain good analog ground planes for minimum jitter performance. The analog ground should be tied to VSSB and VSSI at the DSP56401.

One potential problem can occur when using this circuit with very slow DSP clock frequencies. The DSP56K family DSPs have an maximum SSI clock frequency of one-fourth the DSP clock. If the SSI clock frequency supplied by the DSP56401 is too high for the associated DSP, the DSP will not be able to program the DSP56401. After reset, P18=P19=0, selecting zero input, so the PLL attempts to push the VCO frequency downwards. But P20=P21=0 after reset, selecting non-inverting polarity, so the VCO frequency is actually forced upwards to its upper limit. The PRC clock frequency after reset is OSCIN0 ÷ 4 so if PRC is connected directly to the SSI clock, the DSP clock frequency must be equal to or greater than the maximum OSCIN0 frequency. The PTC clock frequency after reset is OSCIN0 ÷ 8, so if PTC is connected directly to the SSI clock, the DSP clock frequency must be equal to or greater than one-half the maximum OSCIN0 frequency. This is only a problem after reset and before program bits have been loaded.

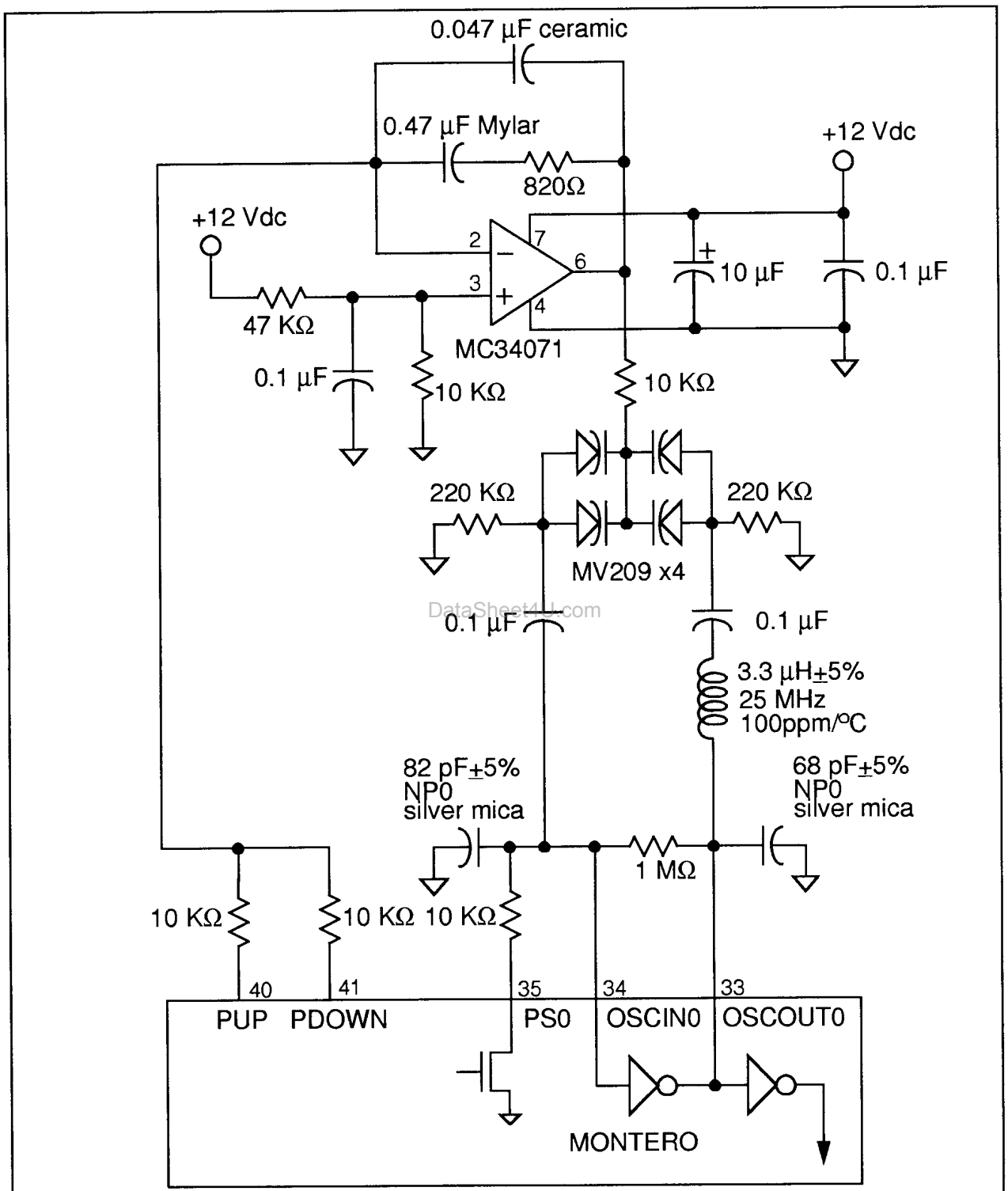


Figure 8-10 Voltage Controlled LC Oscillator (24 MHz)